NON-LITHOGRAPHIC AND SCALABLE MANUFACTURING OF SILICON MICRO & NANOMATERIALS

BY

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DISSERTATION

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Abstract

In the last decade, accelerated discovery of novel processing schemes has enabled rapid prototyping and large volume production of parts with extended and programmable functionality - such as biodegradable electronics, high-emissivity surfaces, optoelectronics circuits, fast-discharging batteries, meta-materials, energy conversion systems, and light-weight composites. Novel micro/nanomanufacturing methods - such as 2D and 3D printing, imprinting, self-assembly, deterministic micro-assembly, flexography, and roll-to-roll systems - are among a growing set of new platforms that allow for integration of metals, polymers, oxides, composites, nanomaterials and biomaterials hierarchically across length scales ranging from centimeters down to nanometers. However, nanomanufacturing platforms are still plagued by a trade-off between throughput and resolution, ultimately hindering the scaling of nanomaterial production.

In this context, this thesis introduces two novel processes for manufacturing hybrid and hierarchical silicon nanomaterials: (a) 1D nanostructure fabrication via thin-film dewetting and electrochemical etching, and (b) arbitrary-shaped 3D surfaces via direct electrochemical imprinting. Uniquely, they offer 3D dimensional control with sub-20 nm lateral and vertical resolution, mirror surface finish (i.e. RMS < 5 nm), high-aspect ratio (i.e. >20), low-defect density (i.e. no porous formation), and large-area patterning (>1 cm^2). In each of these approaches, a fundamental understanding of ionic diffusion, reaction kinetics, and nucleation dynamics are directly correlated to manufacturing outputs - such as morphology defect density, material removal rate, patterning fidelity and resolution. Three scientific contributions have been made to the existing literature: (a) correlating electrochemical rate of reduction and oxidation to

sidewall profiling in catalyst-based etching of silicon, (b) evidencing of diffusion limitations in solid metal catalysts, and (c) measuring the effect of porous substrate and catalysts in controlling the morphology of MACE-fabricated nanostructures. Overall, the techniques developed in this thesis bypass the need for dry etching and lithography, and are potentially compatible with amorphous and polycystalline silicon and III-V semiconductors. In turn, they may pave the way for the manufacturing of complex 3D hybrid objects on semiconductors for use in microoptics and nanophotonics, energy harvesting, and biosensing.

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I dedicate this work to my beloved parents who have taught me to live in “the here and the now”, to do my best every day gratefully, not more or less than what I am capable of.

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Chapter 1. Introduction

Today, nanomanufacturing research addresses the challenge of shaping, integrating and functionalizing nanomaterials. Since the inception of the Silicon Valley, the use of nanotechnology expanded beyond well-established industries such as integrated circuits (IC), photovoltaics (PV) and microelectromechanical systems (MEMS). This expansion was enabled by the discoveries of 0D, 1D, 2D and 3D nanomaterials such as quantum dots (QDs) [1], carbon nanotubes and silicon nanowires (SiNWs) [2], graphene [3], and photonic crystals [4] (Figure 1). In the early 1990's and 2000's, it was shown that such nanomaterials possess dramatically different mechanical, chemical, optical, thermal, electrical, and magnetic properties as compared to its bulk counterpart. In turn, engineers have proposed to harvest such unique properties into functional nanodevices for applications in computing, energy [5], food sciences [6], defense, and medicine [7].

For commercial development, these early device concepts demanded that manufacturing processes and platforms be radically rethought to address the manufacturability [8, 9], safety [10, 11], sustainability [12] and costs of nanomaterials. For example, in 2008, single-crystal electronic-grade SiNWs manufactured onto a wafer were first proposed as a high-capacity electrode for lithium ion batteries to replace standard graphitic anodes [5]. To commercialize such innovation, it would require, at a minimum, to scale production volumes of SiNWs from laboratory scale (i.e. micrograms) to production scale (i.e. tons). In an optimistic scenario, processing of SiNWs via top-down or bottom-up microfabrication approaches can only

manufacture SiNWs at a rate of 0.02 Kg/hour per wafer[1]. With the battery market demanding 125,000 tons/year of battery-grade graphite[2], it would require a minimum of one million wafer processing lines to match such demand levels. In addition, SiNWs would also have to achieve cost parity with battery-grade graphite (currently priced at ~ 3 USD/Kg). With the bulk cost of metal-grade and electronic-grade polysilicon at 2 USD/Kg and 25 USD/Kg[3], respectively, there is little to no room for additional processing costs. This is a classic example of the scalability and cost barriers that nanomaterials face in order to transition into commercial development.

Another critical requirement of conceptual nanoscale devices is that multiple materials (i.e. polymers, metals or ceramics) and its unique functionalities must be seemingly integrated to perform coordinated functions [13]. At the micro and nanoscale, this integration poses manufacturing challenges as it requires selection of materials that are compatible with each other and its associated processing steps. In the first case, distinct materials are referred to as "incompatible" if they react or degrade upon contact. For example, the growth of single-crystal III-V semiconductors onto silicon wafers leads to excessive crystal defects due to lattice mismatch, ultimately degrading its electronic and optical properties [14]. In the second case, distinct materials cannot be processed together due to an inability to withstand shared processing conditions (i.e. heat, chemical environment, pressure). This is typically the case for materials with dramatically different thermal or chemical properties. For instance, low-melting point materials will often sublimate if processed at elevated temperatures which is often

[1] Calculated throughput by assuming the run-time only of SiNW fabrication onto a 300 mm wafer with dry-etching. Dry-etching rate is estimated as 2 µm/min. Note that this argument considers dry-etching as the limiting-rate step and ignores other intermediate steps such as lithography.
[2] According to Benchmark Minerals, news article, 2016.
[3] According to PV consulting, public report, 2013.

required for high-melting point materials. Thus, manufacturing integration of distinct materials often requires one to select alternate materials and processes so that they can co-exist without significant degradation.

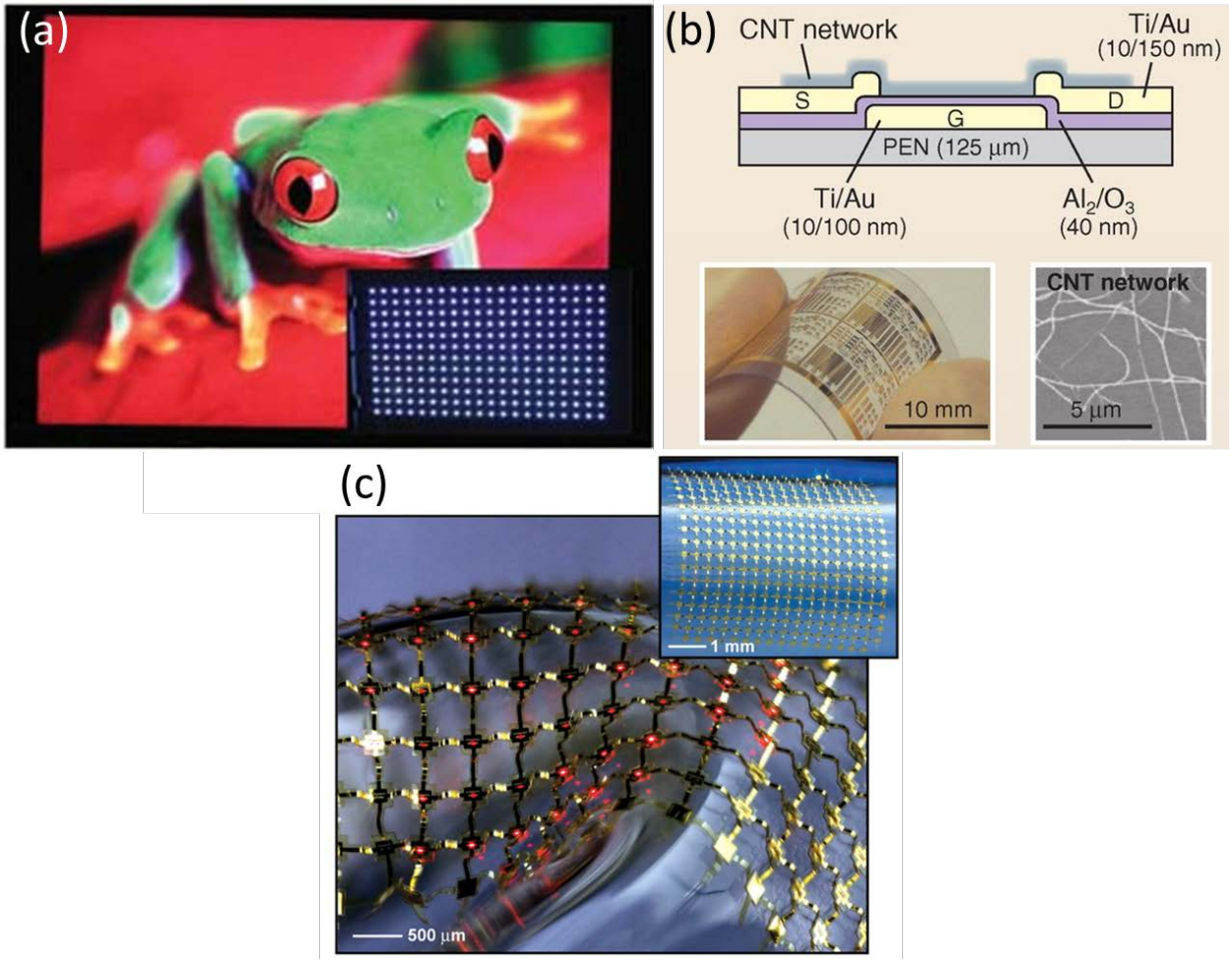

Figure 1: Examples of multi-materials hierarchically integrated into functional devices. (a) Display image of a 46 inch LCD TV panel and a quarter of the white QD-LED backlights (inset), adapted with permission from literature [1]. Copyright (2010) Advanced Materials. (b) Flexible TFTs using CNT networks deposited by aerosol CVD, adapted with permission from literature [2]. Copyright (2013) Science. (c) Passive matrix, stretchable ILED display that uses a noncoplanar mesh configuration, on a rubber substrate, adapted with permission from literature [13]. Copyright (2009) Science.

In summary, often times, every new breakthrough device in nanotechnology that is demonstrated on a laboratory faces uncertainty and risks in its pathway to commercialization due to manufacturing challenges. In turn, it pushes the limits of our current nanomanufacturing

capabilities and motivates researchers to explore new strategies to (a) scale nanomaterial production volume by several orders of magnitude, (b) to improve geometrical control, (c) minimize defects during fabrication processes, and (d) integrate multi-materials in hierarchical architectures.

1.1 Motivation

Within the context of micro and nanomanufacturing, two distinct topics are motivated below which are nanomaterial synthesis and multi-material integration. The subsections below, "Silicon Nanomaterials: Application-Driven Manufacturing Challenges" and "Silicon Hybrid Nanomaterials: Multi-Material Integration", elaborate on specific problems motivating the work presented in chapters Chapter 3, 0 & Chapter 5.

1.1.1 Silicon Nanomaterials: Application-Driven Manufacturing Challenges

Among an increasing variety of materials, silicon is still an attractive option since it is one of the most abundant elements on the earth's crust. Further, nanostructured forms of silicon have enhanced chemical, optical, thermal and electrical properties as compared to its bulk counterpart. For instance, silicon nanowires are theoretically the highest capacity and most durable anode for lithium-ion batteries [5]; silicon microlenses can accurately manipulate the wave front of light beams in miniaturized systems used in silicon photonics and bio-imagining [15, 16, 17]; microstructured porous silicon is a biocompatible and biodegradable material for integrated bioelectronics, targeted drug delivery and chemical sensing [18, 19, 20, 21, 22, 23]. Common to all of these applications is the challenge of nanostructuring silicon in a scalable, sustainable and low-cost fashion.

Strategies for manufacturing these key silicon nanomaterials were largely inherited from the semiconductor industry. Realizing the challenge of microstructuring this brittle material, industry adopted the idea that silicon is patterned indirectly by a series of chemical and mechanical steps. First, a 2D template, typically a thin-film, is defined onto the surface of a silicon wafer and, subsequently, the substrate is patterned via top-down (i.e. etching) or bottom-up (i.e. growth) methods (Figure 2 – "Indirect Patterning"). A combination of high-resolution methods for patterning the template (such as EUV lithography) and etching or growing silicon yielded patterning capabilities at the micro and nanoscale. While this platform achieved a high degree of parallelization, it suffers from low dimensionality in geometric control (i.e. 2.5D only), and finite part volume (i.e. aspect ratio). Further, the inability to reuse the template generates unnecessary waste and increases cost. This indirect lithographic approach has remained the benchmark platform for silicon nanomanufacturing until today.

1.1.2 Silicon Hybrid Nanomaterials: Multi-Material Integration and Applications

The use of silicon nanomaterials in a greater realm of applications is possible when it does not function alone. When successfully integrated with other nanomaterials that can perform complementary functions, silicon hybrid structures – such as silicon nanowires decorated with nanoparticles - perform key functions in solar energy harvesting [24], biomolecular sensing [25, 26, 27, 28, 29], and cancer cell annihilation [30, 31]. In such example, metal nanoparticles are responsible for localizing surface plasmons which produces light absorption enhancements and improves photochemical energy conversion [32] while high-aspect ratio nanowires offer large surface area, and unique optical and electrical properties [33]. This hierarchical and multi-

material structure successfully integrates the functionalities of semiconductors and metals. However, existing techniques for nanoparticle decoration onto 1D elements offer restricted control over particular size and shape, ultimately restricting the design space [31, 25, 34, 26]. Alternative methods for the synthesis of metal nanoparticles onto 1D nanostructures are needed that can fine tune the nanoparticle morphology characteristics (i.e. size, density, spacing, shape, contact angle).

1.2 Thesis Outline

In summary, two key issues of silicon nanomaterial production and integration have been raised thus far: (a) silicon nanostructures are still manufactured via indirect parallel methods, and (b) techniques for forming silicon-containing hybrid nanomaterials offer limited morphological control. This thesis tackles these two limitations by (i) introducing novel methods for non-lithographically fabricating silicon 1D and 3D micro and nanoscale features, and (ii) integrating silicon nanowires with metal nanoparticles, respectively. This is achieved by introducing a new self-assembly and nonlithographic method for fabricating 1D silicon nanomaterials, an electrochemical imprinting method for nanopatterning 3D features onto silicon and porous silicon, and a self-assembly method for decorating metal nanoparticles onto 1D high-aspect ratio nanostructures (Figure 2).

The thesis is divided into three chapters that reflect these distinct contributions and are called:
“Chapter Chapter 3: Hierarchical Assembly Of Nanomaterials Via Thin-Film Dewetting”,
“Chapter 0:

Porous Silicon Patterning Via Electrochemical Imprinting", and "Chapter Chapter 5: Silicon Electrochemical Imprinting with the Use of Porous Stamps". Each of these chapters are based on published papers and often repeat phrases, paragraphs and entire segments of these papers [35, 36, 37]. Additionally, the literature review is presented in Chapter 2 and covers a formal and detailed review of existing manufacturing methods for silicon 1D and 3D feature patterning and production, including self-assembly and nonlithographic methods, direct and indirect top-down and bottom-up approaches, and deterministic micro-assembly.

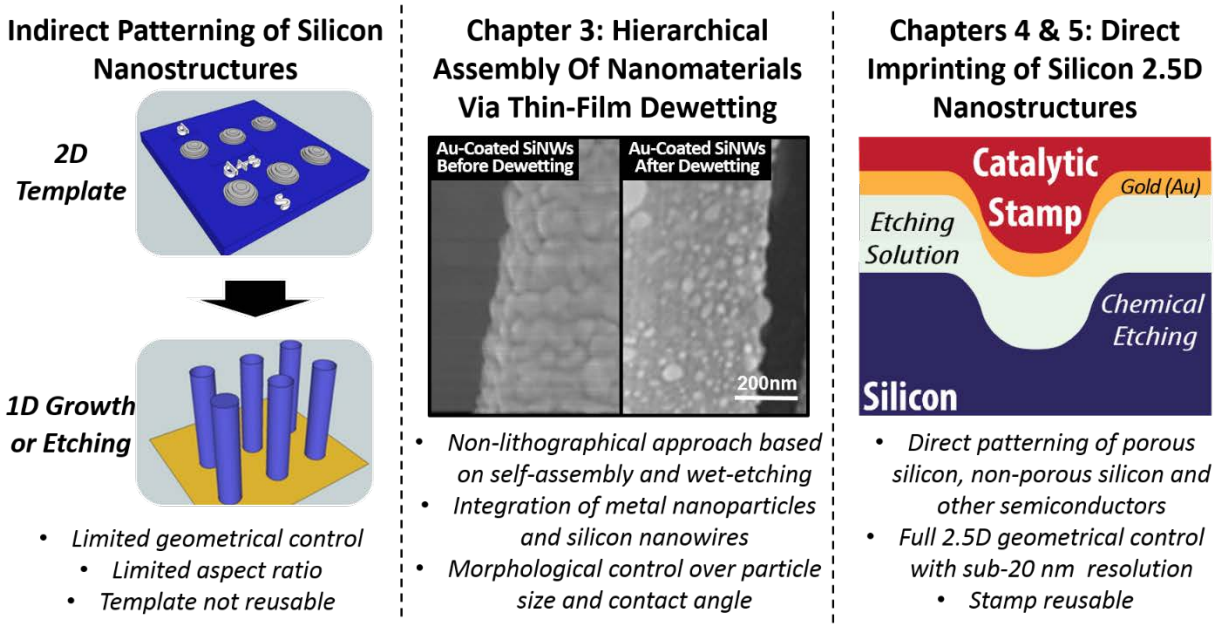

Figure 2: Overview of Thesis Work

1.3 Scope of Research

This section describes the desired performance characteristics and metrics of the proposed manufacturing approaches described in this thesis which is presented in the following sub-sections below.

1.3.1 SiNW Production and Decoration

Chapter 3 highlights the progress made to develop a large scale, non-lithographic manufacturing process for silicon-based thermoelectric devices and anti-reflective surfaces that are environmentally benign, cost-effective, scalable and meet or surpass the efficiency of state-of-art devices. Here are some of the requirements of the SiNW manufacturing and decoration process:

- Create a process flow that is capable of large-area fabrication of SiNWs. The approach is to be free of photolithography and must not require a cleanroom environment
- As a general requirement, the process must be scalable, reproduceable in large-areas (greater than 3 inches in sample size)
- Production of SiNWs arrays with sub-100 nm diameter for thermoelectric devices and sub-300 nm diameter for high-emissivity surfaces
- Rough SiNWs surfaces with controllable RMS roughness in the range of 1-4 nm
- Areal coverage of active material (SiNWs) greater than 40%
- Aspect ratio of active material greater than 10
- Defect-free SiNWs (e.g. no twinning, porosity, or other crystallographic defects)
- Tunable taper angle (smaller than 15˚) with diameter in the range of 200-300 nm and high areal coverage (greater than 30%)

- Nanowire decoration must be able to self-assemble metal catalyst nanoparticles onto the surface of nanowires conformally
- Process for nanoparticle decoration must offer control of particle morphology, specifically size and contact angle, via external inputs

In light of such requirements, the primary goal of this research is to devise a manufacturing strategy that could deliver all desirable metrics. Thus, chapter 3 presents the details of the integration of thin-film metal dewetting and metal-assisted chemical etching used to obtain silicon nanowires with prescribed metrics within the target values such as wire diameter, areal coverage, roughness, taper, aspect ratio and defect level required by the applications. Further, it discusses how to utilize metal-assisted chemical etching to modulate the roughness and taper angle of SiNWs and provides the characterization of the average root-mean-square height variations along the rough wire surface via image analysis of transmission electron microscopy data and the anti-reflective properties of tapered structures. Next, SiNWs are coated in a sputtered gold ultra-thin film that is dewetted to decorate gold nanoparticles onto its surface. The subsequent task was to control the morphology of the dewetted nanoparticles onto the surface of the high-aspect ratio SiNWs which was achieved by varying the annealing temperature during dewetting.

1.3.2 Silicon Nanoimprinting

Chapter 4 and 5 present a proof-of-concept electrochemical nanoimprint method aimed at manufacturing reflective and refractive micro-optical components for the visible range, porous

silicon gas and biosensors and silicon micro-optical components for the infrared regime. In light of such potential applications here a list of the desired characteristics for nanoimprinting:

- Direct porous silicon and silicon nanoimprinting capabilities without the need for lithography and clean-room processing
- 3D dimensional control
- Lateral and vertical resolution in the sub-20 nm with high pattern fidelity
- Surface roughness in the sub-5 nm range
- Fast etch rates (>2 μm/min)
- Minimal morphological damage to substrate such that optical properties of the substrate remain unchanged
- Highly parallell platform calable of large area patterning (> 1 cm^2 for a prototype system and > 900 cm^2 for future industrial systems[4])
- Stamps used imprinting must be reusable (> 20 times in laboratory testing and > 10,000 times for future industrial systems[5])

If such metrics can be achieved, there could exist potential commercial applications of electrochemical nanoimprinting in various industries. Chapters 4 and 5 present extensive data on the relationships between manufacturing inputs and outputs and seeks it to explain these relations to known models in literature.

[4] This is a prediction of the minimum required performance for any future commercial development of electrochemical nanoimprinting of semiconductor materials such as silicon.

[5] Same observation as previous footnote.

Chapter 2. Literature Review

This chapter reviews a wide-span of techniques developed for patterning 3D nanoscale features into semiconductor single-crystal wafers with a strong emphasis on industry's most used material: silicon. Although many of these also apply to amorphous and polycrystalline materials, there is a broader set of techniques for patterning them that is not covered in this chapter. The techniques are classified in a hierarchical tree classification shown in Figure 3 and are meant for the reader to easily identify the strengths and weaknesses of each process.

First, the discussion is organized into two key categories: indirect and direct patterning (i.e. sub-chapters 2.1 and 2.2). Indirect patterning is a class of processes that distinctively use a sacrificial template (i.e. template is not reusable) as a way to assist or mask the subsequent growth or etching of the semiconductor substrate. In contrast, direct patterning is capable of molding, etching or shaping features directly, without the use of sacrificial templates, and assisted only by heat, plastic deformation or etching/deposition techniques.

Secondly, processes are organized in sub-catergories according to the dimensional control (i.e. 2.5D and 3D) and throughput (i.e. parallel or serial) it offers. Most indirect processes offer 2.5D dimensional control with some control over the sidewall profile and are parallel in nature (see sub-chapter 2.1.1). As an exception, a few indirect processes have been specifically developed to address the need for 3D dimensional control which are not necessarily parallel (see sub-chapter 2.1.2). In contrast, all direct processes inherently offer 3D dimensional control, but

thoughput is largely dependent on the serial (see sub-chapter 2.2.1) or parallel (2.2.2) nature of the process.

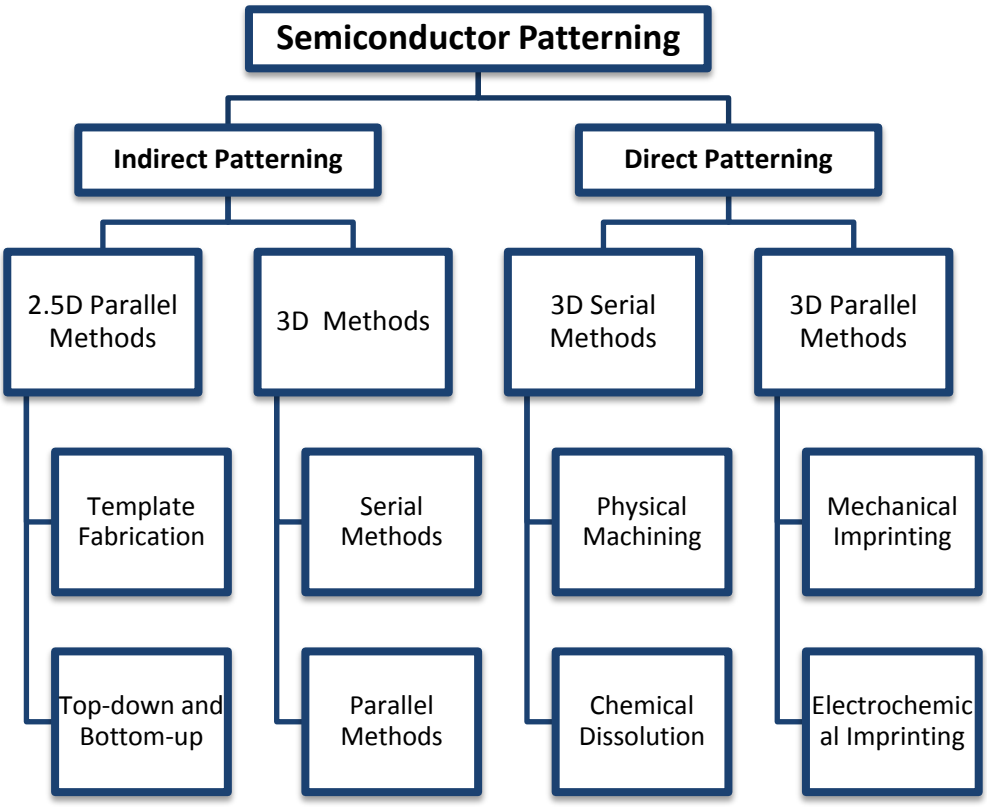

Figure 3: This schematic provides an outline of the literature review as well as a contextualization of the contributions of electrochemical imprinting to semiconductor patterning

2.1 Indirect Semiconductor Patterning Processes

Indirect parallel methods for semiconductor patterning – such as the combination of lithography and etching techniques – were largely inherited from the early days of the semiconductor industry. This indirect approach has achieved three important performance characteristics. First, it induced minimal morphological damage or stresses to the semiconductor substrate, preserving its electronic, optical and mechanical properties. Second, it extended throughput to industrial scales by increasing the degree of parallelization and automation of

manufacturing platforms and processes. Third, additional manufacturing technology improvements - such as immersion exposure for lithography and the Bosch cycle for reactive ion etching [38] - improved lateral resolution down to the sub-20 nm range and enabled 2.5D dimensional control and side-wall profiling [38, 39]. As a direct consequence of these advantages, lithographically defined templates used in combination with etching techniques are now widely adopted in production systems for FinFETs, high-emissivity surfaces, solar cells and MEMS devices.

2.1.1 2.5D Patterning

In every 2.5D patterning process flow, three building blocks are present (see Figure 4). Firstly, a 2-D template is created to define the location, spacing and dimension of SiNWs. Subsequently, the template assists or participates in an out-of-plane growth or etching process, giving SiNWs a prescribed height or depth, respectively. Finally, the last step is to functionalize its surface according to the desired application. This sub-section is organized as to provide an overview of (a) unconventional and emerging techniques for creating 2D templates, and (b) etching and growth methods for silicon 2.5D nanostructures. The functionalization approaches (most of which are chemical treatments used in biosensing applications) abound in the literature and are not covered in the discussion presented in this thesis.

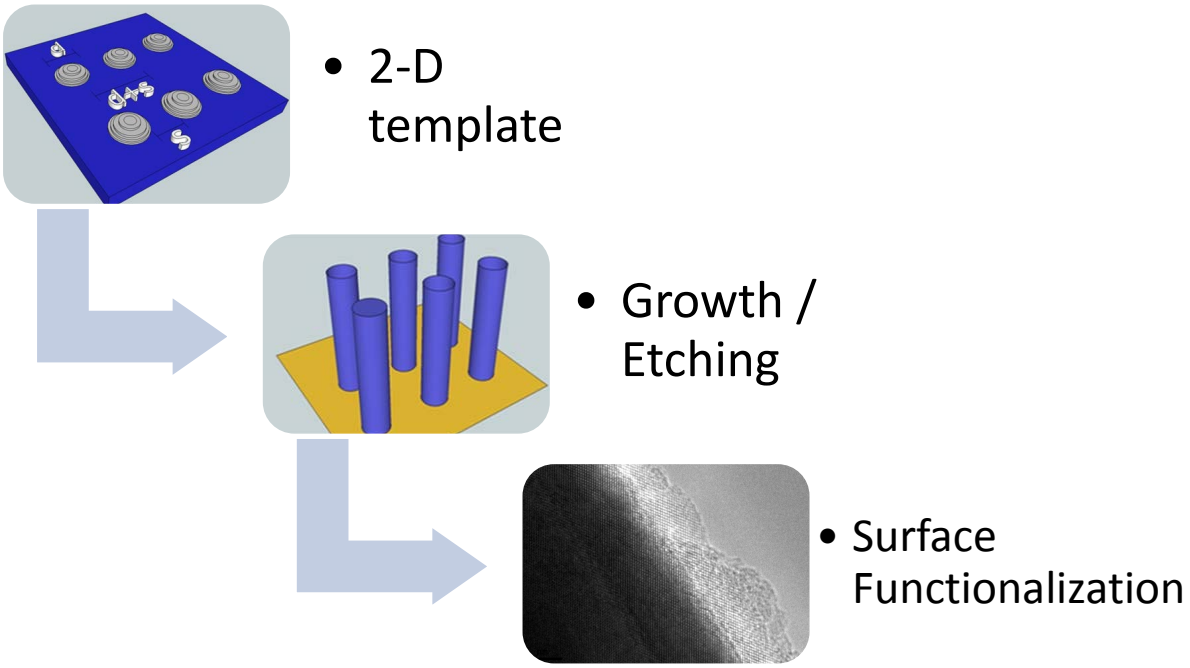

Figure 4: Silicon Nanowire Manufacturing Building Blocks. 2.5D nanoscale features are typically manufactured via a process flow that is comprised of a 2-D template that is defined and used to assist the growth or etching of SiNWs. The last step is optional and is intended to functionalize its surface.

2.1.1.1 2D Templates: Unconventional Non-Lithographical Methods

A template is first defined to mask or catalyze the subsequent growth or etching of silicon nanowires. This section discusses five non-lithographical methods to produce such templates and how they have been integrated with growth and etching methods to produce silicon nanowires.

Direct Method Using Deep-reactive Ion Etch (DRIE)

A direct example of forming a forest of 1-D silicon nanotips was first investigated by Jansen et al., using reactive ion etching (RIE) on a Silicon wafer. The redeposition of polymer masks and adsorption of silicon dioxide particles during the etching step in RIE create micromasks that protect the substrate to form silicon tips (also known as micrograss). The taper profile of these structures was controlled by adjusting pressure, flow of reactive gases, and power of the RIE process [38]. In a single-step, this process can both (1) create the mask for nucleating the tips,

and (2) etch the substrate, creating high-aspect ratio, tapered, and dense arrays of nanotips. More recently, other plasma etching techniques have been developed to yield more robust results for controlling the taper and creating self-masks with higher densities such as pulsed-mode DRIE [39] and electron cyclotron resonance plasma etching [40], respectively. While these approaches are economical and yield samples with low reflectivity in the visible and near-IR range, little work has been done to independently adjust the taper and the density of self-masked patterns which may allow for further reduction in reflectivity.

Nanoparticle Dip Coating Assembly

A typical indirect approach is dip coating with a monolayer of silica beads [41] uses the Langmuir-Blodgett assembly method [42, 43] to produce a close-packed layer of beads over large areas [44, 45]. This step is followed by an isotropic RIE step to separate and shrink the beads starting from a 200-600 nm diameter [45]. Used as a mask over which a thin metal film is deposited, a metallic mesh with monodispersed pores is produced by the removal or lift-off of the beads. This, in turn, is used as catalyst by the MacEtch process to produce SiNW arrays [43]. As-fabricated wires can be shrunk to 60-120 nm by a thermal oxide growth and removed by etching in hydrofluoric acid. However, this approach suffers from the drawback of producing SiNW forests with low areal coverage, detrimental for system-level efficiency of several of the applications previously discussed.

Anodized Aluminum Oxide

Porous anodized aluminum oxide (AAO) [46] with monodispersed pores has also been used for producing SiNWs with the advantage of having highly tunable diameter control in the sub-200nm range. AAO is grown on a bulk aluminum foil [47, 48] or thin-film [49] by a two-step

anodization with the pore depth and size controlled by the anodization time and the pore opening step. Multiple approaches [45, 49, 47] may be used to open up the bottoms of the pores so that the membrane can be used as a template. The AAO membrane is manually transferred to the silicon substrate with the use of a polymeric film as a handle after the Al substrate is etched away [47]. The polymer handle is then removed by dissolving in a solvent. Finally, the closed ends of the AAO pores are opened using an isotropic AAO etchant. AAO membranes – transferred via this method - are covered with an Au film and immersed in MacEtch solution to produce SiNWs. Even though this process integration has been shown to produce SiNWs arrays, the areal coverage of SiNWs produced by this method is limited by the template wall thickness and pore closure effects [47, 48]. Also, the process requires a number of delicate manual steps in the transfer of the template, thus limiting the size of the patterned surface and the yield.

Solid State Superionic Stamping and Metal-Assisted Chemical Etching

A more versatile approach to manufacturing a metal template with a non-photolithographic approach is to use Solid State Superionic Stamping (S4). Since, metal-assisted chemical etching widely uses silver as a catalyst, S4 can be easily integrated with this approach to produce silicon nanowires with sub-150 nm features. Silver features are produced by S4 on a silver thin film deposited onto a silicon wafer and, subsequently etched in metal-assisted chemical etching [50] (Figure 5). However, control over the etching direction and porosity during MacEtch with silver has been an issue due to silver dissolution into ionic form and its redeposition, and the absence of a method to predict or suppress this phenomena.

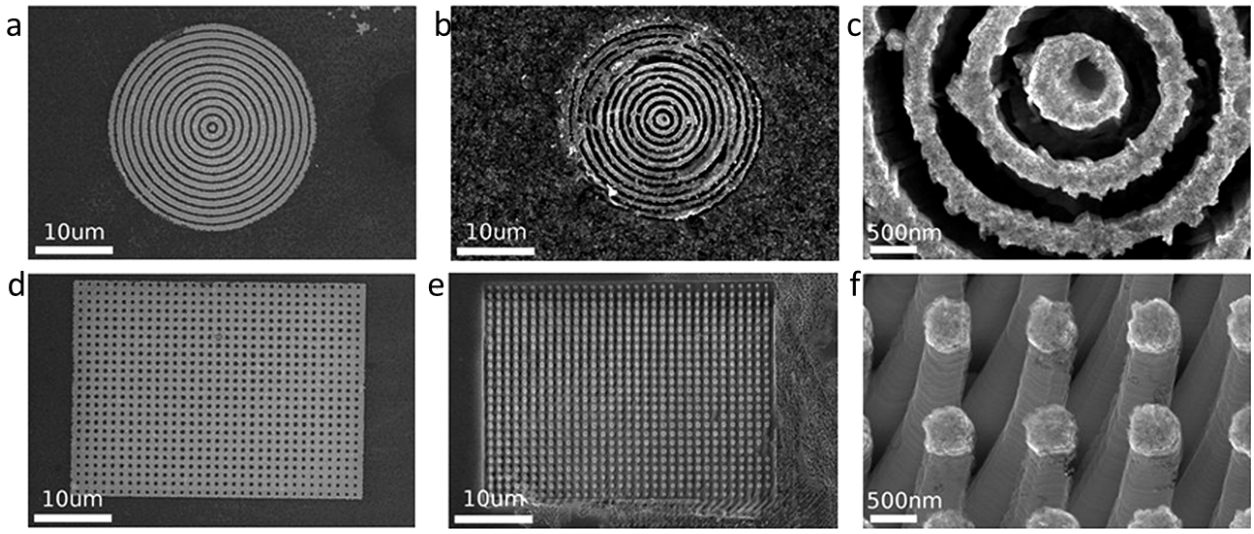

Figure 5: SEM images of S4 patterns (a,d) and its resulting patterns after MacEtch in top view (b,e), and tilted view (c,f) (courtesy of Winston Chern and Dr. Xiuling Li) [50].

Metal Nanoparticle Formation via Thin-film Dewetting

Thin-film dewetting is a scalable and robust process for creating self-assembled monolayers of metal nanoparticles in the 10-500 nm size range on oxide surfaces [51, 52]. A metallic thin-film is first deposited on the substrate. This is followed by a thermal annealing step that activates thermal grooving in the thin film and results in the formation of individual nanoparticles. Unlike approaches that use AAO templates or dip-coating and are capable of producing monodispersed metal particles for MacEtch, this process inherently creates particles with a size distribution with standard deviations starting at 5 nm for sub-20 nm particles and growing up to 40 nm for 150 nm particles. The dewetting behavior has been shown to spontaneously occur for metals such as Ag [52], Co [53], Ni [54, 55], Cu [56], Au [57] and Pt [58]. The annealing temperature to cause dewetting is usually less than a third of the metal's bulk melting temperature. Accelerated diffusion of impurities into semiconductors at elevated

temperatures limits the use of high-melting point metals. Low-temperature options include Ag, Au, Co, and Ni which typically exhibit the dewetting behavior around 300 °C and below 600 °C.

Surface Decoration

There are several methods for self-assembling 0D metal particles onto the surface of semiconducting nanowires: (a) embedded nanocluster formation via rapid thermal chemical vapor deposition [31, 25], (b) electroless plating nanoparticles [27, 59], (c) sputtering, (d) thermal evaporation [60, 61], and (e) atomic layer deposition (ALD) [62]. When combining the functionalities of metals and semiconductors, ensuring the process temperature is below the eutectic points is critical to avoid atomic mixing (via diffusion) and preserve their individual properties. While rapid thermal chemical vapor deposition requires high-temperature processing, all others methods are carried out near RT. Out of a pool of candidates for low-temperature processing, only ALD has been shown to control nanoparticle assembly. As ALD uses costly gas precursors not suitable for large-scale energy applications, alternative methods for the synthesis of 0D metals onto 1D nanostructures are needed that still provide control over nanoparticle morphology characteristics (i.e. size, density, spacing, shape, contact angle).

A straight forward and low-cost approach to self-assembling nanoparticles with control over size and density on a surface is thin-film dewetting. In this approach, a metal, dielectric, or polymer solid thin film is heated to approximately one third of its melting temperature, resulting in the film breaking down into nanostructured patterns [63]. Initially, this breakdown is driven by a competition between grain boundary grooving and grain boundary growth. Edge retraction later becomes the prevalent mechanism that governs the morphology evolution into the final

nanoparticle configuration [63]. By controlling the film thickness and deposition rate, metal nanoparticles with diameters in the range of 10-400 nm can be assembled with independent control over particle size and area density onto flat substrates like quartz and silicon (Si) wafers [35]. While much work has been done to understand dewetting onto low aspect ratio nanostructured surfaces (i.e. templated dewetting) [64, 65], dewetting onto high-aspect ratio nanostructures has not been examined in detail [66, 65].

In addition to thin film dewettting onto high-aspect ratio nanostructures, the control of the particle shape and contact angle during this process is in its nascent form. For example, after the thin film breaks down, gold nanoparticles (Au-np) form a contact angle with the supporting Si surface that is not typically reported as a function of particle size or annealing temperature profile (i.e. temperature ramp rate and set point temperature) [67]. Recent atomistic and experimental studies on vapor-liquid-solid growth reported on the temperature dependence of the composition of Si rich Au-np for a temperature regime above the eutectic temperature (T_E = 636 K) of the Au-Si alloy [68, 69]. In this temperature regime, Si atoms diffuse into the Au lattice to form a superstructure [69]. This behavior can modify the cohesive energy of the particle and thus potentially influence the contact angle. Below the eutectic point, it is uncertain if the contact angle should depend on temperature since the alloy system is technically a solid. No experimental or theoretical studies have investigated this fundamental question thus far.

2.1.1.2 Bottom-up and Top-down Approaches

The most common etching and growth techniques that have been used to produce 2.5D silicon nanostructures includes: deep reactive ion etch (DRIE), vapor-liquid-solid (VLS) growth [70,

71], and metal-assisted chemical etching (MacEtch) [72] in order of decreasing technology readiness. DRIE was developed in the 1990's to serve the microelectronics industry's need for high-aspect ratio structures with fast etching rates and has remained the industry standard since then. VLS growth was invented in the 1960's and it did not receive much attention at the time. It reemerged in 1990's as a method for making silicon nanowires [73]. Today, VLS is still not commercially used due to slow and size-dependent growth rates, and little control over growth direction. In 1993, early literature on electroless etching of silicon by hydrofluoric acid solutions proposed that selective etching of silicon was possible by the use of a metal template [74, 75]. Later, in 2000, this process was coined MacEtch by the work of Professors Xiuling Li and Paul Bohn. Since then, it has received much attention due to its ability to create silicon features with sub-5 nm resolution [76], and aspect-ratios greater than 100. Over the last decade, MacEtch literature has matured but it has yet to see a commercial application. The following section discusses the advancements made in the last decade on this later technique.

Metal-Assisted Chemical Etching

Metal-assisted chemical etching (MacEtch) is a process in which a mixture of HF and an oxidant (typically H_2O_2) is used to etch a semiconductor such as Si in the presence of metal [77]. The process works by injecting a hole into the semiconductor from the reduction of an oxidant at the metal-solution interface. Then, the availability of holes in the vicinity of the semiconductor-metal interface triggers a reaction between surface silicon atoms and hydrofluoric acid through one of the proposed mechanisms in literature [78]. In the case of hydrogen peroxide as oxidant, the most accepted mechanism in literature is the reduction of hydrogen peroxide into water and an electron-hole followed by its injection into the valance band of silicon. Subsequently, electron-

holes are consumed in the dissolution of silicon by hydrofluoric acid transforming silicon into a water-soluble product called hexafluorosilic acid (H_2SiF_6). The reactions steps are shown below:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+$$

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

The balance between hole injection and consumption maintains holes localized at the metal-substrate interface and, consequently, directional etching is achieved with non-porous single crystalline features being generated. When deployed in SiNW fabrication, MacEtch produces nanowires with aspect ratios greater than 100 [79], provided the diffusion of reactants and products to and from the reaction zone is abundant. For this reason, MacEtch has been widely used for generating dense and vertically aligned nanowires for integration with planar manufacturing processes [80].

In regards to porosity control of SiNWs, MacEtch has been demonstrated to produce solid or porous features by controlling the ratio of the oxidizer concentration to that of HF [51] and by changing the catalyst metal [50]. Previous work [81], reproduced on Figure 7a, demonstrates that the etch rate peaks when the value of a parameter *ρ*, defined as a molar ratio, is in the range 70-80%, where:

$$\rho = \frac{[HF]}{[HF]+[oxidizer]}$$

In this range, the rate of reduction of hydrogen peroxide is stoichiometrically balanced to the rate of oxidation of silicon underneath the catalyst. Increased oxidizing activity produces

excess holes which are injected into Si and transported to the SiNW boundary. The presence of holes at the SiNW surface as it is formed makes it susceptible to chemical dissolution by HF and causes roughening of the surface of the nanowire followed by the growth of a porous layer on the shell of the nanowire that progresses toward its core as the etches progresses in time (see Figure 7b-c).

The rate-limiting mechanism for the dissolution of silicon is the diffusion of either reactants or products towards or away from the metal-semiconductor interface, respectively. Dr. Nadine Geyer and collaborators working at the Max Plank Institute proposed and verified a diffusion model in which the pathway for reactants and products takes place around the edges of the catalyst layer (Model II in Figure 6) and not through it as previously proposed in literature (Model I in Figure 6). Furthermore, it was verified that MacEtch works by first creating a thin Si porous layer under the catalyst until it reaches a uniform and stable porous thickness that allows for the diffusion of reactants and products as the etching progresses in time. When the feature size of the catalyst layer is in the order of sub-500 nm, the diffusion lengths are small and the thickness of this porous layer is thin to the point that it is hard to observe it in the silicon nanowire samples produced in this thesis. However, in theory, it exists and is fundamental for the progress of the etching. Another consequence of this model is that the rate of oxidation of silicon at the vicinity of the metal-semiconductor junction is dependent on the length that ions have to diffuse through and, consequently, dependent upon the feature size. Thus, when implementing metal-assisted chemical etching, one should never take the solution parameter ρ reported elsewhere and assume it is universal and will yield equal morphological results for all catalyst geometries. Instead, one should choose a parameter near and above the value corresponding to the peak in

etch rate. Porous layers under the catalyst may grow as large as several microns before it reaches a steady state thickness for the case of features sizes greater than one micron, approximately.

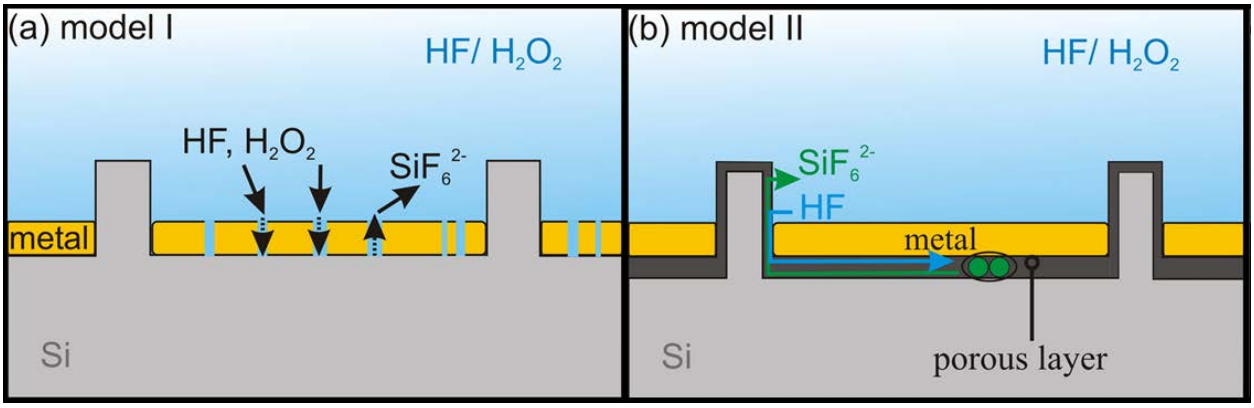

Figure 6: Scheme of possible diffusion processes of the reactants and reaction products during metal-assisted chemical etching. (a) Model I: Diffusion of reactants and reaction products through a porous thin metal film. (b) Model II: The oxidation of the Si surface proceeds at the interface of the metal and the Si substrate by forming a porous silicon layer. Through the porous layer, the HF can diffuse to the bulk Si to facilitate the dissolution. The reactants and the byproducts diffuse as well through the porous layer. Adapted with permission from literature [78]. Copyright (2012) American Chemical Society.

In regards to morphology control of SiNWs, MacEtch can achieve some roughness control of its sidewall profile by decreasing the parameter ρ or, similarly, adding more hydrogen peroxide. Our previous work [51] shows that RMS roughness can be controlled only in the 0.5-2 nm range. Beyond 2 nm, the wire roughening becomes so aggressive that it results in the formation of porous SiNWs, significantly reducing their electrical conductivity. The same mechanism for roughness generation can also be used for tuning the taper of its sidewall feature. For instance, further increasing the oxidizing activity accelerates the side-wall porous formation and its subsequent dissolution in HF, resulting in a tapered external profile [81] (see Figure 7d). This approach, unfortunately, also causes the core of the SiNW to be porous for most levels of useful roughening and tapering.

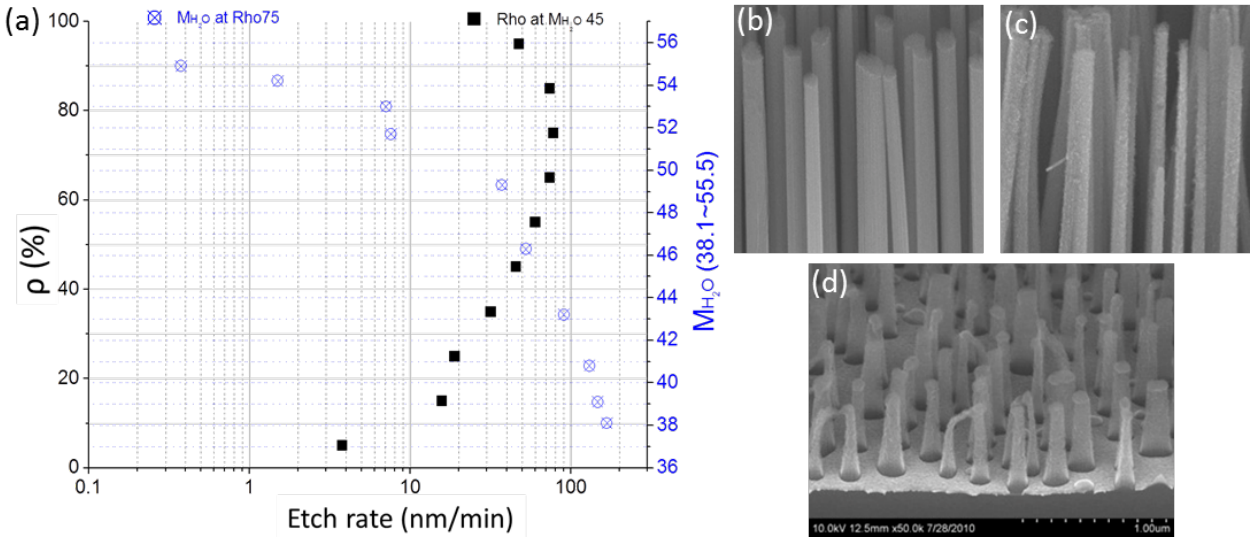

Figure 7: 4: (a) the etch rate of Macetch is characterized as a function of the etch parameter (ρ) and as a function of water molarity for a catalyst mesh with areal coverage of 22% and average hole diameter of 120nm. These results are partially reproduced from literature [81]. In figures (b) and (c), the sidewall morphology of the tips of silicon nanowires portrayed by SEM images are smooth and rough according to the etch parameter chosen: 75 and 65, respectively [51]. An evident taper (d) is observed at etch parameter typically in the range of 55 and below.

2.1.2 3D Patterning

Expanding patterning capabilities from 2.5D into 3D can potentially increase the realm of devices that may be mass produced by indirect parallel processes towards plasmonics, nanophotonics, optics, micro and nanofluidics, and biosensing. In light of this opportunity, grayscale lithography was first developed in 1995 [82] to tackle the challenge of shaping polymeric materials in 3D. The "grayscale" term refers to the spatial modulation of the exposure dosage of photons, electrons or ions. In the case of photons, exposure dosage controls the cross-linking through the depth of a photo-curable film; parallel grayscale methods uses gray-tone masks [83] and DMD maskless exposure systems [84, 85, 86] and harvest this mechanism to produce features with lateral and vertical resolution around 1 µm.

Later, nanoimprint lithography (NIL) [87, 88, 89] was invented and it enabled the achievement of sub-10 nm resolution in 3D by the use of mechanical imprintation of soft materials. NIL allows for fast pattern replication from a 3D hard master mold, which is typically fabricated by serial methods such as micro-stereo- [90, 91], two-photon [92, 93], grayscale e-beam [94] or grayscale ion-beam lithography [95].

Irrespective of how the template is produced, it must still be indirectly translated into the underlying semiconductor substrate by standard dry and wet etching methods. However, this process combination has been far from trivial and resolution is lost due to (a) error propagation due to the indirect nature of this approach, (b) error amplification due to high etching selectivity of template and substrate, (c) non-uniformities in template and substrate erosion, and (d) scalloping induced during the Bosch cycle (as depicted in Figure 8).

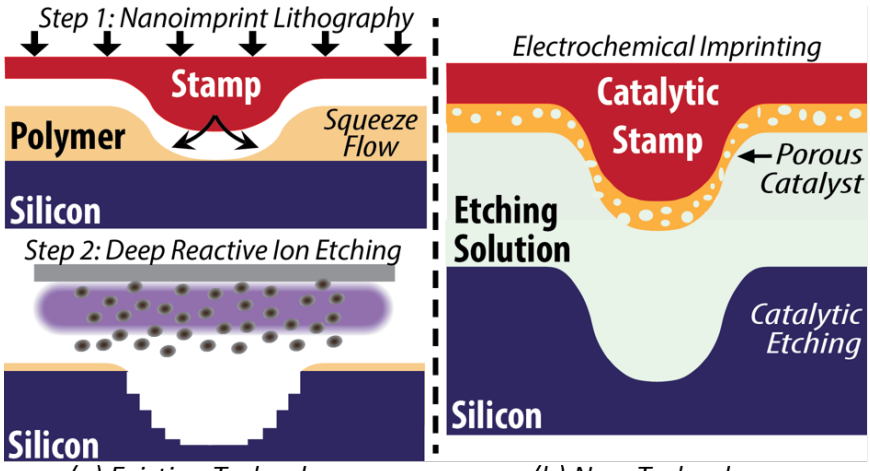

Figure 8: Schematics of a typical indirect (left) and direct (right) route to semiconductor patterning. The indirect route depicted is the combination of nanoimprint lithography and DRIE. The direct route depicted is the electrochemical imprinting approach introduced in chapter 4 and 5 of this thesis. The schematics highlights the scalloping effects of DRIE, and error propagation and amplification of indirect routes.

2.2 Direct Semiconductor Patterning Processes

The attractive characteristic of direct methods is that, by definition, they bypass the need for the use of templates, and, as a result, can potentially reduce costs associated with non-direct processes such as photolithography, and, thus, may potentially scale production of nanomaterials. Most direct methods offer some degree of 3D control with varying resolution, substrate damage and throughput. In this context, a review is presented of the performance characteristics of serial and parallel methods.

2.2.1 Serial methods

Most serial-writing methods are intrinsically capable of 3D dimensional control – such as laser [96] and electrochemical [97] machining - and sub-20 nm resolution in 3D via ion-beam milling [95]. However, due to its slow throughput rate, serial methods have been primarily used for master mold fabrication and prototyping in research and development environments. The selection of a serial method is based on a trade-off between throughput and resolution which is often tied to the physical mechanism governing the material removal. For instance, laser machining has the fastest throughput among serial methods; through the use of high-energy femtosecond pulsed lasers, it induces local surface melting and recrystallization, and, thus generates undesirable crystal defects and stress fields. Further, the diffraction limit and heat dissipation on the material contribute to lowering its resolution as well.

Another example is ion-beam milling which has the slowest throughput, and, by controlling the spot size and energy of input ions, it can reach an unprecedented sub-20 nm resolution in certain materials. Finally, electrochemical machining relies on nanosecond electrical

pulses and the instantaneous charging of the double layer to localize an electrochemical reaction to the toll-substrate interface. As a result, its throughput is limited by the reaction rate at the tool-substrate interface and diffusion of reacting species. Additionally, it generates significant porous defects on semiconductor substrates around the feature, limiting its resolution to the microscale. Thus, it is still incredibly difficult to pattern semiconductor nanostructures with 3D dimensional control and sub-20 nm resolution while maintaining the substrate morphology intact.

2.2.2 Parallel Methods: Imprinting

State of the art nanoimprinting methods enable parallel patterning of silicon, porous silicon and many other materials such as metals and polymers. Each of these methods exploits different mechanisms for material removal and flow. As such, the subsections below review two sub-categories: mechanical and electrochemical-based processes.

2.2.2.1 Mechanical Imprinting Processes

Nanoimprinting technique for silicon was first proposed by Chou, Keimel and Gu in 2002 and was coined as LADI which is an acronym for “laser-assisted direct imprint” [98]. As the name suggests, LADI uses a 308 nm nanosecond pulsed laser that passes through a transparent quartz mold in contact with a silicon wafer. At this wavelength, silicon completely absorbs this wavelength of light within a 300 nm penetration depth. In turn, this thin-layer melts instantaneously for a period of hundreds of nanoseconds and, upon action of the stamp, it reflows during its molten stage into the quartz mold. The mold and substrate are demolded and the mold may be reused in subsequent imprinting operations [98]. While this approach achieved

sub-100 nm in a parallel and fast fashion, it produced structures with limited depth – limited by the heat localization to surface layers – and substantial morphological damage induced by recrystallization during cooling and impurity incorporation, which, ultimately "changes [silicon] from a semiconductor to a metal" [98]. At the same time, this approach is widely extendable to other materials such as metals [99] and also works at temperatures below its melting temperature by embossing which relies on the plastic deformation of the material in its solid phase [100].

Interestingly, specific mechanical-based nanoimpriting methods have been invented to pattern porous silicon and other porous materials mostly motivated with the idea to preserve the crystallinity and existing morphology of porous materials highly sensitive to heat-based strategies. Two methods stand out and are reviewed here: dry-removal soft-lithography (DWSL) [101] and direct imprinting of porous silicon (DIPS) [102, 103]. In common, they exploit the controlled fracturing or collapsing of the porous material to selectively strip or compress porous silicon. Stress concentrations at the pore walls enables its fracture that does not propagate throughout the remainder of the material and, thus, remains confined to the dimension of the pore wall. While DWSL is restricted to 2D patterning with microscale resolution, DIPS can generate 3D features with sub-100 nm resolution. DIPS relies on the compaction of porous silicon leading to permanent deformation of the substrate and, thus, modifying spatially the porous morphology and the optical properties of the substrate. While this characteristic can be advantageous for certain applications, a low-stress patterning method that does not damage the pore morphology is yet to be demonstrated. The attractive characteristic of DIPS is that (a) it operates at room temperature and largely preserves the original crystal morphology of the

substrate and (b) it applies for all porous materials, enabling patterning for a much wider class of materials such as porous metals and polymers.

2.2.2.2 Electrochemical Imprinting Processes

Electrochemical nanoimprinting processes for silicon had not been invented prior to the work elaborated for this thesis. The closest analogous process of an electrochemical-based imprinting process is solid state superionic stamping (S4). S4 is a non-photolithographic process that electrochemically dissolves silver thin films into silver ions in the contact areas between an ionic conductive stamp and a metal substrate (Figure 10). Metal ions are transported into the solid electrolyte stamp by an applied bias and reduce on the back of the stamp. This stamp-based approach can produce sub-100 nm Ag features at high-throughput rates [104].

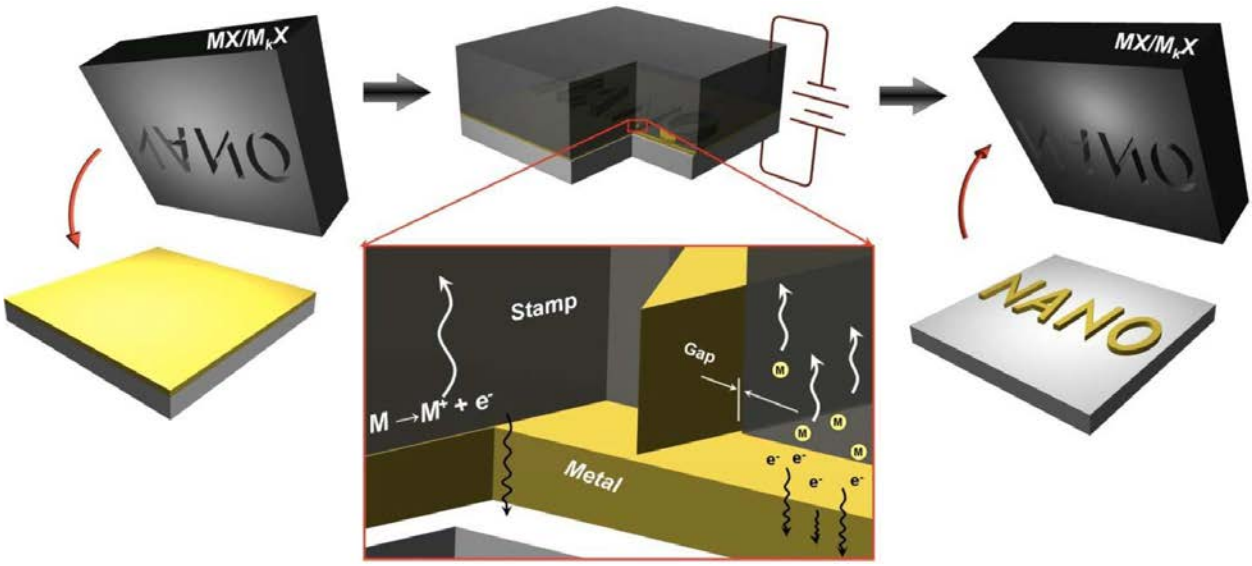

Figure 9: Schematic of solid state superionic stamping process. Left: A patterned stamp of superionic conductor—of M+ ions—is pressed against a film of metal M. Center: A small applied voltage anodically dissolves metal in contact with stamp; M+ ions are absorbed into the electrolyte. Right: Removal of metal continues eventually reproducing the relief patterns from the stamp in the remaining metal (courtesy of Kyle Jacobs) [104, 105].

Chapter 3. Hierarchical Assembly Of Nanomaterials Via Thin-Film Dewetting

In this chapter, a fabrication scheme for obtaining SiNW arrays with controlled sidewall morphology, size distribution and density is reported. In addition, decoration of SiNWs by gold nanoparticles is presented thereafter. To fabricate SiNWs, our approach begins with silver (Ag) thin-film thermal dewetting in which a sub-15nm layer of evaporated silver film is heated to induce dewetting of silver onto a silicon substrate. Then, gold (Au) is deposited over the silver nanoparticles and the particles are removed by a metal lift-off technique to generate a large-scale Au mesh on Si substrates. Followed by metal-assisted chemical etching (MacEtch), where the Au mesh serves as catalyst, arrays of smooth Si nanowires are produced. By fine control of the deposition rate and thickness of the evaporated Ag film that is dewetting into Ag nanoparticles, SiNW arrays with average diameter as small as 61nm with a standard deviation of 13 nm are produced. Further, it is shown that, by altering the chemical composition of the MacEtch solution, tapered wires are also produced. Additionally, this chapter introduces an approach to produce SiNWs with surface roughness fine-tuned in the 0.5-3.5 nm range consistently across the wire length. To accomplish this, an additional post-roughening step is used. As-formed SiNWs are coated with Au nanoparticles via sputtering and etched by MacEtch again. Au nanoparticles etch toward the core of SiNWs. Roughness control is obtained by controlling the etching time. After roughening, the SiNW surface develops a native oxide and the Si/SiO_2 interface roughness is characterized by TEM.

After synthesis of a wafer-scale array of SiNWs, it was sought to decorate such structures with gold nanoparticles with controlled morphology. In the selected approach, a conformal ultra-thin film (i.e. < 15 nm thick) is deposited onto SiNWs and thermally dewetted, forming nanoparticles in the 6-70 nm range. Two parameters of its morphology are dependent upon dewetting conditions: particle size and particle contact angle. Using transmission electron microscopy (TEM) imaging, it is found that annealing temperature profile has a strong effect on the particle size. Additionally, the contact angle is found to be dependent on particle size and temperature even below the eutectic temperature of the Si-Au alloy. Molecular dynamics simulations were performed by collaborators at Purdue (i.e. Mike Sangid) to investigate potential explanations for such experimental observation. In this temperature regime, the simulations reveal the formation of an amorphous phase at the interface between the catalyst and SiNW that is sensitive to temperature. This amorphous layer increases the adhesion energy at the interface and explains the contact angle dependence on temperature.

This work may enable a deeper understanding of the relationships between (a) roughness and thermal conductivity of SiNWs, (b) taper and reflectivity of tapered SiNWs, and (c) nanoparticle morphology and catalytic properties of decorated silicon nanowires. Further, the approaches explored are readily scalable and can potentially be implemented in large-scale manufacturing of SiNWs for thermoelectric devices, tapered silicon nanotips for high-emissivity surfaces for stray light reduction in telescopes, and Au-decorated SiNWs as electrodes for artificial photosynthesis.

3.1 Silicon Nanowire Fabrication Via Thin-Film Dewetting

Two sets of samples were manufactured for the purpose of investigating the roughness dependence on MacEtch parameters and the broadband anti-reflective properties of tapered SiNWs. The first set was comprised of smooth SiNWs with average diameter in the 110-140 nm range that were roughened to various levels and analyzed under TEM. The second set is comprised of as-doped and post-doped tapered SiNWs with average diameter around 300 nm.

3.1.1 Particle Size Control via Dewetting Parameters

The process begins by growing a 15nm oxide layer on degreased and RCA-1 cleaned (100) Si wafers (1-10 ohm.cm) in a Lindberg Hevi-Duty Lancer M-300 Tube Furnace at 1000 ˚C for 13 min with a 4 sccm pure oxygen flow rate. Subsequently, silver deposition was performed in a Temescal E-Beam Evaporation System with thickness and deposition rate monitored by a quartz crystal monitor (Figure 10a: step 1). Silver films are then annealed at 350 ˚C in rapid thermal annealing chamber that focuses an infrared light source on the sample (model SSA-P610C, manufactured by ULVAC-RIKO, Inc) for 4 hours at 3-8×10^{-7} torr (Figure 10a: step 2); at the end of this step, the Ag film is fully dewetted into isolated particles (Figure 10b). For sub-100 nm particles, we used scanning electron microscopy (SEM) to characterize the particle size distribution as a function of the deposition thickness at a deposition rate as low as 0.1 Å/s. The SEM data is analyzed with ImageJ (see Figure 41) and results for the average particle diameter and areal coverage are shown in Figure 12 as a function of the deposition parameters. Parameters for the 100-400 nm particle size range were reproduced from previous studies [52].

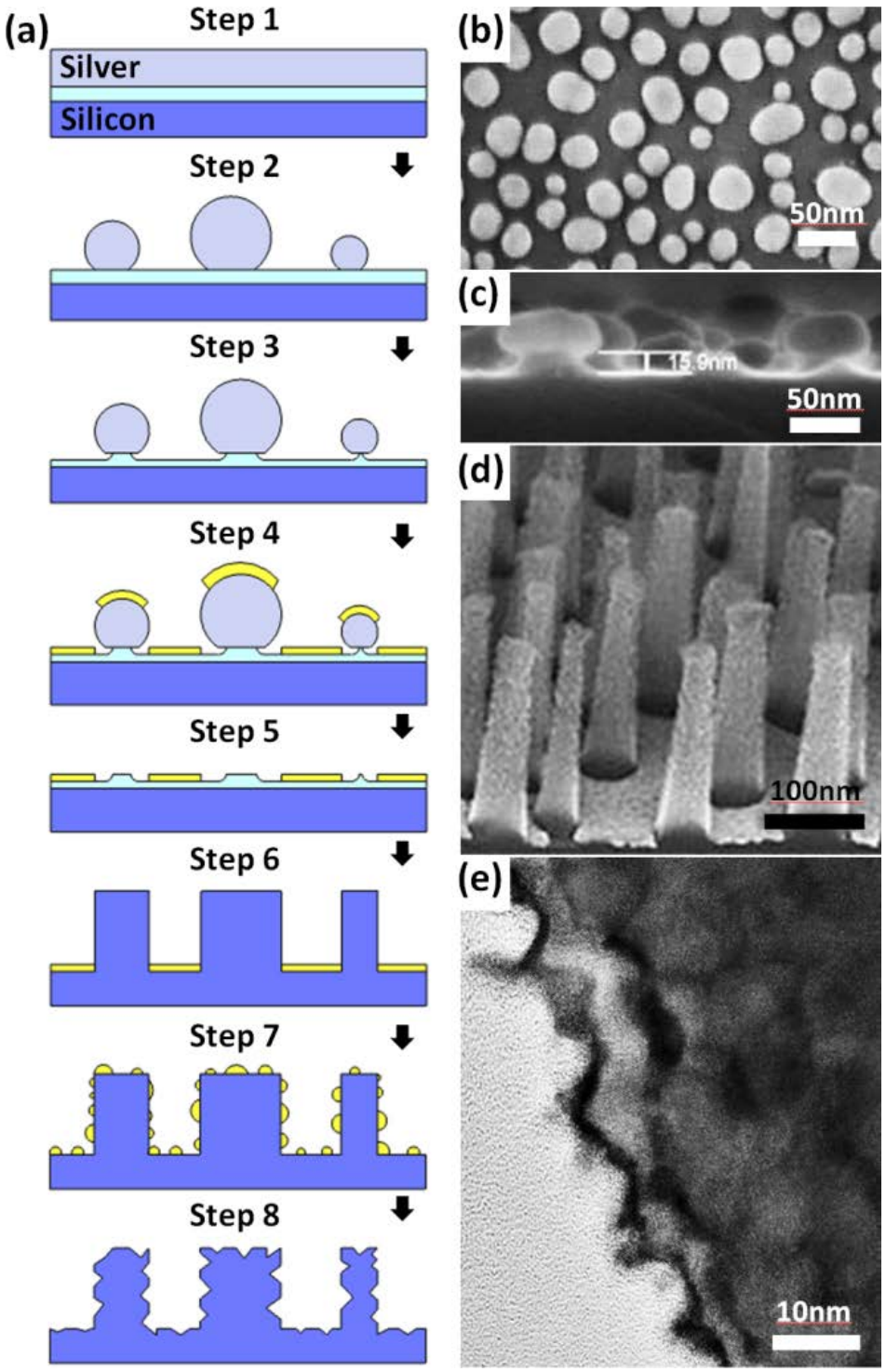

Figure 10: (a) Fabrication overview: silver films are evaporated onto a clean 15 nm thick thermally grown SiO_2 surface at controlled deposition rate and thickness (step 1) (b), thin-films are annealed in vacuum breaking into individual particles (step 2), sub-120 nm Ag particles are undercut with BOE to increase its height and facilitate lift-off (step 3) (c), thin Au catalyst layer is evaporated (step 4), Ag nanoparticles are etched away at room temperature with silver etchant solution (step 5), MacEtch at different ethanol concentrations produce straight and tapered SiNWs (step 6) (d), and Au nanoparticles are sputtered (step 7) and etched in diluted MacEtch solution to generate surface roughness (step 8) (e).

Samples are immersed in a buffered oxide etch ($HF:NH_4F$ = 6:1; v:v) for 20 seconds in an ice bath with temperature kept at 0 ˚C with constant agitation (Figure 7a: step 3). This step undercuts the oxide film under the silver particles and facilitates the subsequent lift-off process (Figure 7c). As observed from cross-section SEM images, the undercut depth was controlled with etching time (Figure 11). Theoretically, 1% HF could also be used to achieve even slower undercut rate [106]. It is particularly important for sub-120nm particles and unnecessary otherwise.

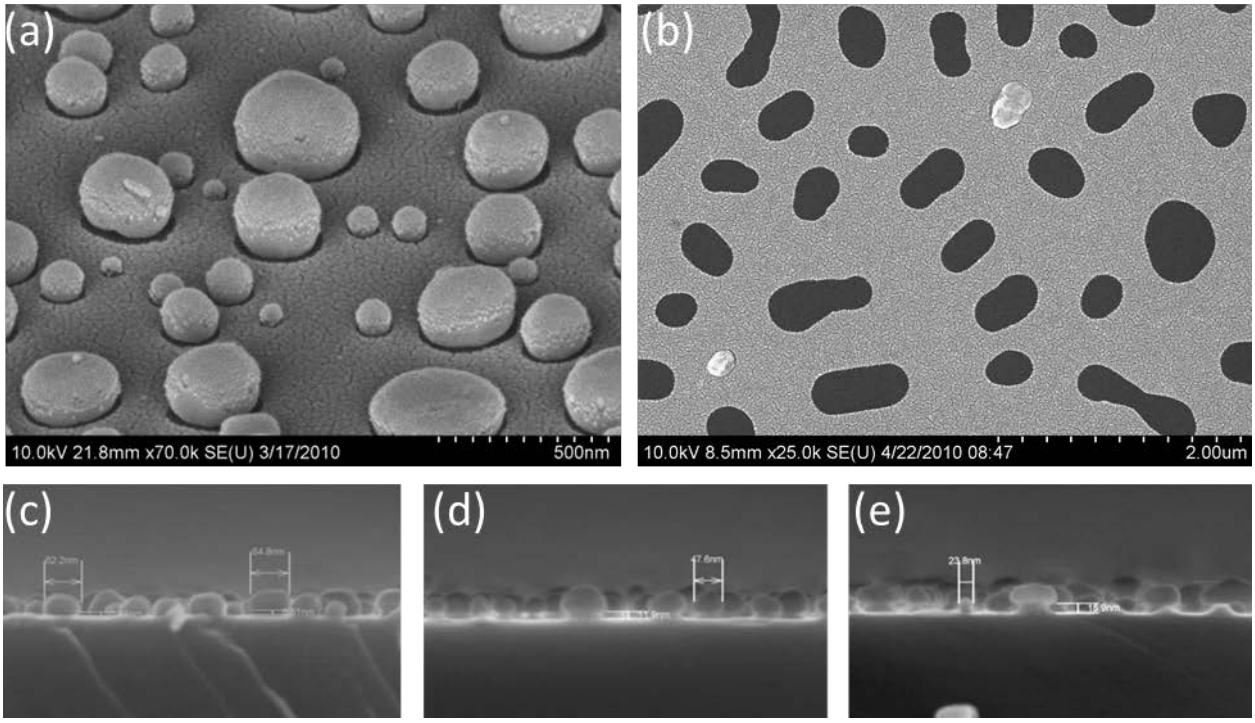

Figure 11: Tilted scanning electron micrographs of samples before (a) and after (b) lift-off step in ultrasonic bath. Also, to improve the lift-off of smaller particles, BOE undercut was performed. The cross-section of silicon substrates covered by thermally dewetted silver nanoparticles and undercut by buffered oxide etch at 0 °C for 10s (c), 20s (d), and 30s (e) are shown.

Next, all samples are evaporated with 10 nm Au at 0.5 Å/s in the same e-beam evaporation system (Figure 10a: step 4), immersed in a RCA-1 solution ($NH_4OH:H_2O_2$:Methanol = 1:1:2; v:v:v) at room temperature and sonicated four times for 10min in each round. After

sonication in RCA-1, most silver nanoparticles covered with Au have been etched (Figure 10a: step 5), leaving behind a gold mesh pattern on the substrate. The gold mesh is now used as the catalyst template for MacEtch (Figure 10a: step 6).

3.1.2 MacEtch: Straight vs. Tapered Wires

The Si substrates with the patterned Au mesh are etched in MacEtch to produce straight (HF(49%):H_2O_2(30%):Ethanol = 13:2:19; v:v:v) and tapered (HF(49%):H_2O_2(30%):Ethanol = 13:2:X; v:v:v) SiNWs (Figure 10d), in which "X" represents the volume ratio of added 99.9% Ethanol to the mixture. For this work, solutions are always made fresh before each experiment and used immediately within 10min. To understand the effect of ethanol concentration on taper formation, the volume ratio of ethanol (X) was varied from 56 to 110 at a fixed 13:2 volumetric ratio of HF(49%) and H_2O_2(30%). Samples were cleaved and we studied their cross-sections in a SEM, measuring the taper of the wires produced. The taper of the wires is constant throughout its height for all cases which indicates that the local rates of hole injection and consumption are constant. This observation leads to the conclusion that the reactants' concentration do not decay during the etching. Additionally, MacEtch etch rates are reported constant for several hours in other papers [77]. From the analysis of the SEM data, we found that the external taper angle of SiNWs increases for solutions with higher ethanol concentration and detailed information is shown in Figure 13 (and in Figure).

3.1.3 SiNW Roughening

The next step to roughen the wire surface was to deposit Au nanoparticles on a set of straight SiNWs samples - 1 µm long with average diameter between 110-140 nm by sputtering on a Denton Desk II TSC (power was set at 20% for 15 seconds). All-angle rotation was activated to uniformly coat the nanowire surfaces (Figure 10a: step 7). At that point, samples were cleaved into 1 cm^2 pieces and SiNWs were roughened (Figure 10a: step 8) by a second etch step that involved immersing the samples in dilute MacEtch solution ($HF(49\%):H_2O_2(30\%):H_2O$ = 1:1:24; v:v:v) for different durations of time, ranging from 5 to 25 seconds. Subsequently, samples were immersed in aqua regia ($HNO_3(68\%):HCl(37\%)$ = 1:3; v:v) for 3 min to remove the Au mesh.

The sidewall roughness of the samples was characterized by high-resolution transmission electron microscopy (HRTEM) (Figure. 7e) and the RMS roughness is plotted as a function of the duration of the roughening etch step shown on step 8 in Figure 10a. High resolution images of the Si/SiO_2 boundary are obtained by tilting the nanowire to [110] zone-axis angstrom level resolution. Several HRTEM images recorded continuously along the length of a nanowire are seamlessly stitched together to generate the roughness profile of the nanowire over a length of ~500 nm. This procedure was conducted for three nanowires from each array to obtain an average RMS roughness for each sample.

3.1.4 Tapered SiNW for Anti-reflection Measurements

For investigating light reflection, two sets of straight and tapered SiNWs samples with a 300 nm average diameter were fabricated using MacEtch. Tapered samples were made with 13.4 Mol/L ethanol concentration. The first set contained wires that were straight and tapered with

lengths of 2 µm and 1.5 µm, respectively. For the second set, tapered wires with lengths set at 11 µm were boron doped in a diffusion chamber with a boron diffusion source (BN-975, Saint-Gobain Ceramics) for 40 min at temperatures of 900 ˚C and 1000 ˚C. The reflectivity in the visible and near-IR range of the first (Figure 17a) and second (Figure 17b) sets was obtained in a Cary 5000 spectrophotometer.

3.1.5 Characterization of Silicon Nanowires

In this section, the results for particle size control of dewetted silver patterns, sidewall taper control of SiNWs, post-roughness generation, and reflection measurements are presented and discussed in the context of the applications and existing literature.

3.1.6 SiNW Fabrication and Taper Control

It has been shown that dewetting of an Ag thin-film can result in nanoparticles with diameters in the size range of 10-80 nm and with area coverage in the 32-42% range. This is related to the changes in thin-film nucleation and growth kinetics as a result of selecting a deposition rate as well film thickness [52]. The nucleation process during evaporation produces peaks and valleys on the thin-film top surface, centered at the nucleation site and the mid-point between them, respectively. These peaks and valleys on the film surface serve as the initial condition for dewetting upon exposure of the film to elevated temperatures. The initial shape favors thermal grooving at the valley region (grain boundary), resulting in the formation of particles centered at their nucleation sites. For a given temperature cycle, the nucleation density for silver island formation on a substrate during dewetting remains the same as that of silver grain formation during deposition. This is shown to be inversely proportional to the incoming flux

of atoms during deposition [52]. This allows us to obtain high area coverage (particle density) at low evaporation rates (Figure 12). In the same figure, the average diameter increases with thickness and we observe a peak in the area coverage. This slight decrease in area coverage as the deposition thickness increases is due to merged grains during dewetting. This is possible because the thermal grooving process becomes less efficient at completely separating nucleation sites as the film thickness increases. This also causes the resulting particles to lose their circular shape, and the resulting particle density to decrease.

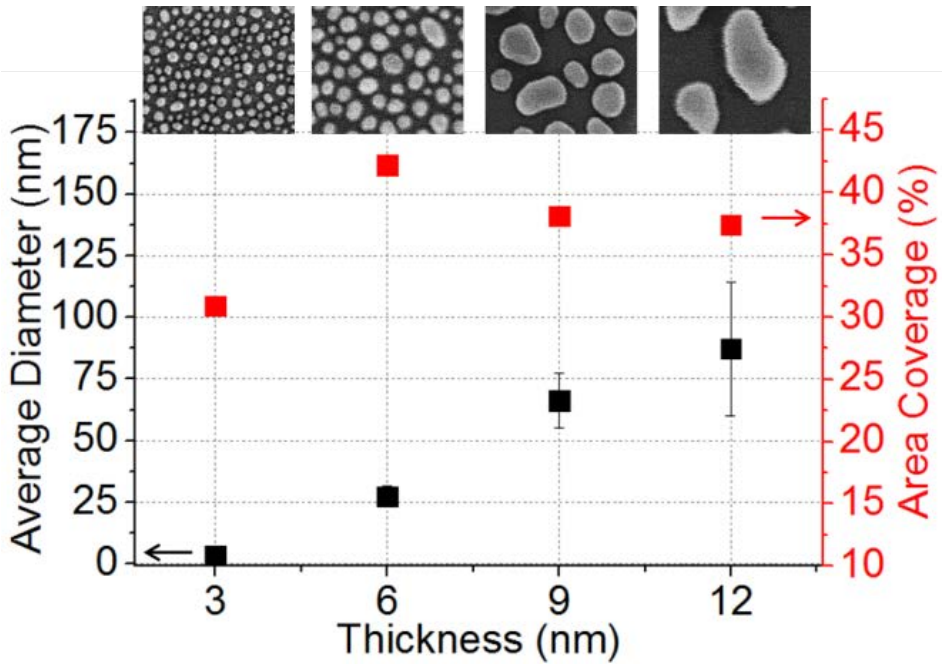

Figure 12: Characterization of sub-100 nm average Ag particle size: (black) average diameter (error bars represent one standard deviation of the wire diameter distribution) and area coverage (red) as a function of film thickness at constant 0.1 Å/s. The SEM images on the top represent each data point at the same magnification.

In the fabrication process, the limiting step for producing SiNWs from the dewetted sub-100 nm Ag particles via MacEtch is the metal lift-off technique described in section 4.1. For this regime, the particle's height is small and less than twice the Au film thickness. Therefore, many particles are coated by Au resulting in a low lift-off yield. To address this issue, we use a BOE

(Buffered Oxide Etch) step to etch the oxide layer that was deposited before the Ag film. This increases the height of the particles by an additional 10-15 nm and also undercuts the oxide under the silver particles to produce pedestal-like structures that greatly facilitate the lift-off process. The smallest reproducible average diameters over 1 cm^2 samples were 61 nm at 22% area coverage and 67 nm at 46 % area coverage (see Appendix A: Silicon nanowire diameter distribution analysis). Further improvements such as decreasing the Au grain size and its thickness are being investigated to fine tune the lift-off yield for even smaller diameters.

Silicon wire tapering is possible by adding ethanol and changing its concentration in the MacEtch solution. The flux of holes injected into the band structure of Si is generated from the H_2O_2 reduction at the Au-MacEtch solution interface (cathode). When excess holes– not consumed by the anodic Si dissolution reaction at the Si-Au interface – become available, they diffuse and migrate away from the Si-Au interface, toward the rest of the Si surface exposed to the etchant. The presence of excess holes in Si near the wires' surfaces increases the rate of SiO_2 formation at the surface. This is subsequently etched by HF [81] to create a porous Si layer. Continuation of this process results in growth of the pores, the loss of the outer surfaces layer, and the extension of the porous layer towards the center of the wires. The tips of the wires, having been created first, are subjected to this process for the longest time and hence the wires develop a taper. The thickness of the porous Si layer on the already formed wires increases monotonically with time. As a result of this, the tips of the nanowires have the thickest porous layer as compared to the bottom of the wire (Figures 10a and 10b). A similar observation has been made by Chartier et al. [81]. In their study of Si MacEtch with Au nanoparticles as catalysts, they found that decreasing the molar concentration of HF relative to H_2O_2 produces a porous

tapered sidewall. The characterization of the external taper angle versus ethanol concentration is shown in Figure 13c. While the addition of ethanol can create controllable wire tapering, this effect was not observed when water was used instead of ethanol to dilute the solution.

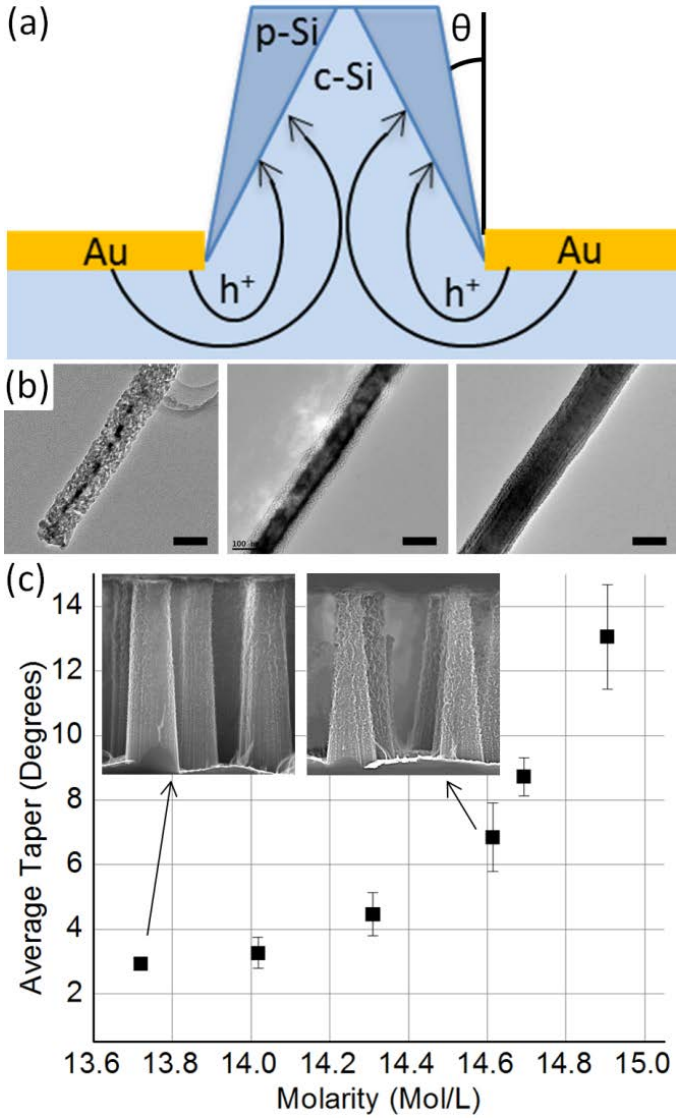

Figure 13: Taper Control: (a) schematics of hole diffusion and migration towards SiNW shell surface, showing external angle, θ, (b) TEM images of the tip through base (from left to right, respectively) of a SiNW etched in MacEtch in [EtOH]=13.4 M, (c) dependence of taper angle on ethanol molarity on solution. Scale bars are 100nm in length.

As described earlier when excess holes become available, the process described above can result in tapered SiNWs. From the overall reaction's perspective [77], excess holes can

become available by two means: an increase in hole generation on the cathode (Au-etchant interface), or a decrease in the rate at which holes are consumed on the anode (Au-Si interface). Our observations indicate that while the water addition reduces the kinetic rates of the cathode and anode reactions equally, the addition of ethanol reduces preferentially the hole consumption rate on the anode. As a result of this, excess amount of holes can migrate from the anode (Au-Si interface).

3.1.7 TEM characterization of roughness dependence on etching time

In the roughening approach, the catalyst is composed of Au nanoparticles that penetrate a few nanometers into the core direction of the nanowires etching a variety of crystallographic planes towards the SiNW core, causing the reformation of the Si and SiO_2 surfaces (Figure 14). Since the penetration path is small, we do not observe any coherence or preferred crystallographic direction in the etching done by the nanoparticles. TEM imaging followed by image analysis reveals the longitudinal topography and surface roughness of the nanowires and the Si and SiO_2 interface. Control over RMS roughness height is attained in the 0.5-3.5 nm range by controlling the etch time (Figure 14a). Successful control of the roughness levels by timed etches is a result of using diluted MacEtch solutions as elaborated in section 3.4.

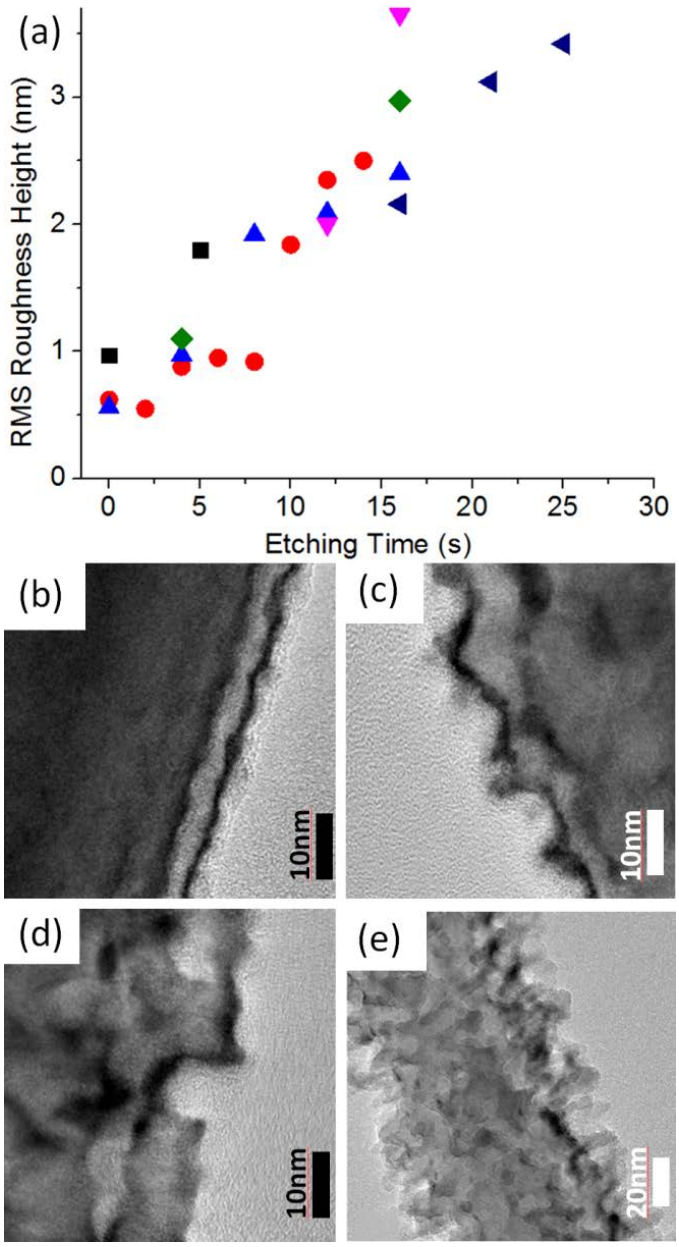

Figure 14: Post-roughening characterization: (a) RMS height as a function of roughening time in diluted MacEtch solution, and low-magnification TEM images of SiNWs: (b) as-prepared, and after (c) 5 s, (d) 10 s, and (e) 20 s of roughening.

3.1.8 Discussion on Porosity Generated by MacEtch

We compared the etch chemistry (Figure 15a, $\rho = 35\%$) employed in a recent study to roughen SiNWs [107] and study its effect on thermal conductivity, and found the tips of nanowires to be relatively smoother and well-defined under high-magnification SEM regardless

of the water molarity at $\rho = 75\%$ (Figure 15b-c) [108]. Since porosity has adverse effect on thermal conductivity, it is important to use the correct ratio.

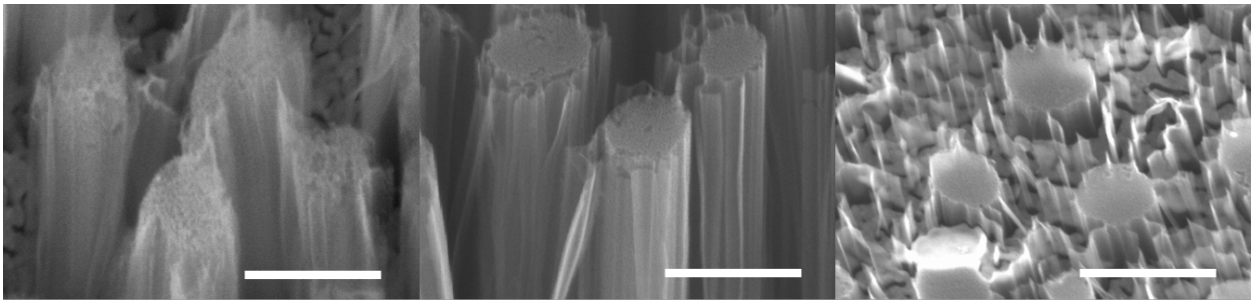

Figure 15: The morphology of the tip of the silicon nanowires is depicted under SEM as a function of etch parameter used to make silicon nanowires. From left to right, the images depict samples etched for 40 s, 40 s and 80 s. The scale bars are 250 nm.

Additionally, it is fundamental to increase surface roughness of nanowires in a controllable manner to further decrease its thermal conductivity below the Casimir limit. Particularly, it was necessary to investigate diluted Macetch chemistries to reduce the etch rate while not creating porosity on the wires. Thus, a separate set of silicon substrates patterned with the Au mesh were immersed in solutions with $\rho = 75\%$ while varying the water molarity from 38.1 M to 54.9 M. The etch rates were measured from SEM cross-section data. The wires are straight for all cases and the tip of the wires produced with diluted solutions remains sharp and seems to not be attacked by the slow Macetch process (see Figure 16). This finding is evidence that the ratio between the rates of the cathodic and anodic reactions remains constant and that the ρ parameter accurately predicts the porosity of diluted macetch solutions for this given geometry of the catalyst. Also, this finding permitted the development of the roughening MacEtch recipe used with the samples shown in Figure 14.

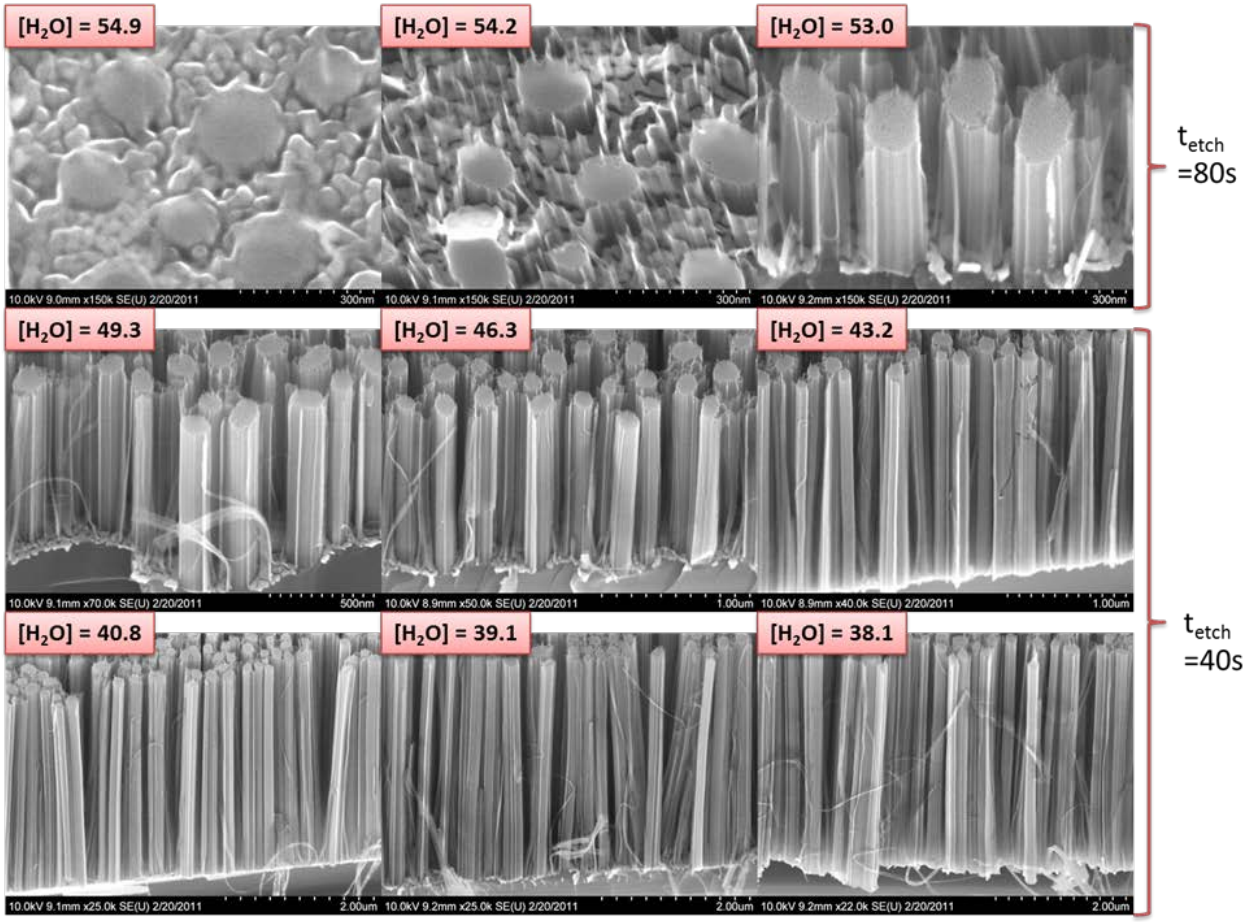

Figure 16: Slow etching in MacEtch. Pre-patterned silicon substrates etched in solutions with $\rho = 75\%$ while varying the water molarity from 38.1 M to 54.9 M show no indication of porosity at the sidewalls or tips. By changing the molarity from $M_{H_2O} = 38.1\ M$ to $M_{H_2O} = 54.2\ M$, we further reduced the etch rate from 108 nm/s to 0.5 nm/s, respectively (see Appendix C).

3.1.9 Anti-reflective properties of tapered and doped SiNWs

Firstly, it is necessary to compare the reflectivity characteristics of straight and tapered structures in the visible and near-IR range. The effect of a slightly tapered SiNWs is captured in Figure 17a. A smooth transition in the refractive index derived from tapered nanowires reduces the reflectivity in the visible range by 77% (particularly around wavelength of 700 nm) relative to straight nanowires for samples with similar lengths. This is possible due to the subwavelength scale of the SiNWs. In the visible range, the reflectivity spectrum for tapered SiNW agrees well

with studies on anti-reflection of silicon nanotips of equivalent length [40]. Beyond the band gab wavelength, light travels into the sample and it is not well absorbed due to the low absorption coefficient of low-doped Si. As a result, light reflects from the back of the wafer and, thus, we observe a jump in reflectivity.

Increasing absorption in the near-IR becomes fundamental to reduce reflectivity in this range. One approach is to increase doping level. Higher doping concentrations facilitate phonon-assisted absorption around the band gap wavelength [109, 110] and increase free carrier density [111]. Both of these effects contribute to lower the reflectivity in our measurements. Figure 17b shows the effect of doping on anti-reflection of tapered SiNWs as a function of the temperature in which the boron doping was carried on.

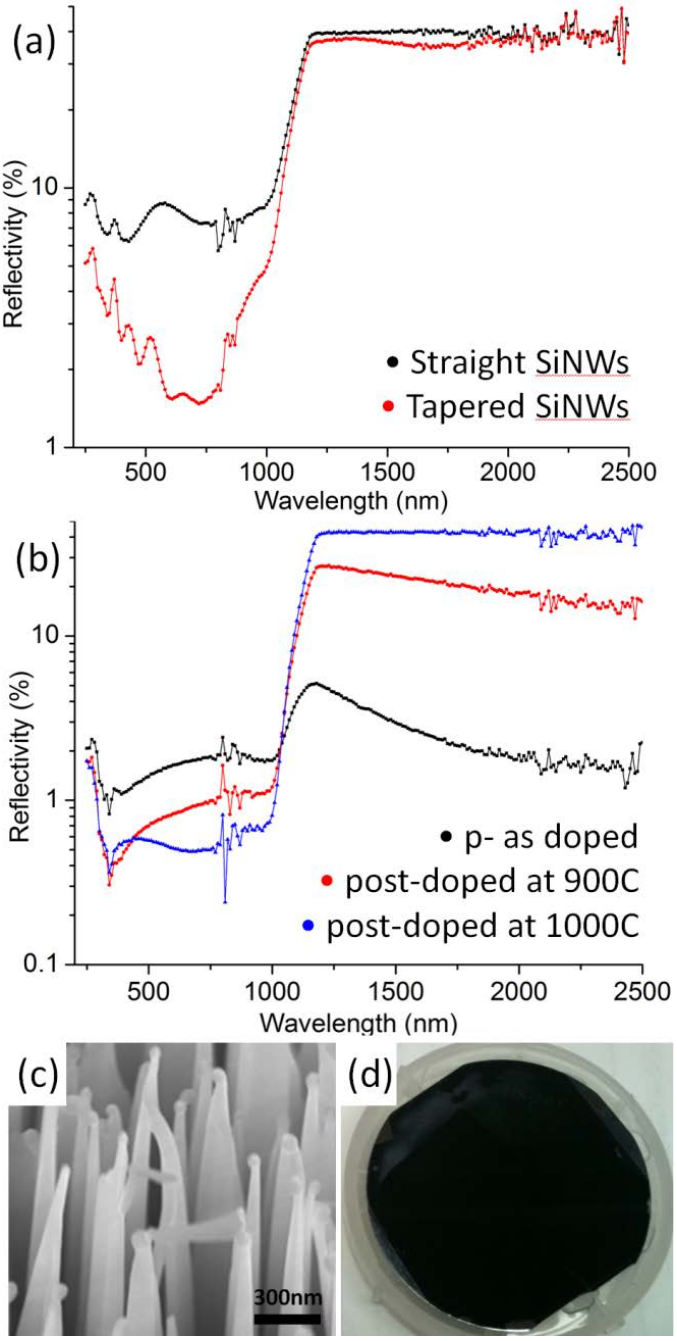

Figure 17: Reflectivity of (a) straigth 2 µm long (black) and tapered 1.5 µm long (red) SiNW and (b) of tapered 11 µm long SiNWs with different doping conditions: 1-10 ohm p-type (reference, blue), post-doped at 900 ˚C for 35 min (red), post-doped at 1000 ˚C for 35 min: instrumental noise was significant at 800-900 nm and 2000-2500 nm but does not obscure data trend; (c) SEM of post-doped SiNWs post-doped at 1000 ˚C; (d) photograph of sample fabricated on a 2 in wafer.

3.1.10 Template Fabrication via Solid State Superionic Stamping

In this chapter, the S4 process was reproduced from literature [112, 104, 113, 114, 115, 116] using Ag_2S stamps and focus-ion beam (FIB) lithography to define nanoscale features. These features were reproduced onto silver films (Figure 18a-b) which were deposited onto silicon substrates. The Ag features were coated in a sub-10 nm thick layer of gold and submitted to the lift-off procedure in sonication as described in section 3, resulting in a patterned mesh of gold. For the first set of samples, 15 arrays of 50 x 50 µm were produced with varying dot size from 180 nm to 1 µm and etched in MacEtch to produce wires (Figure 18b-f). The etch depth was around 25-30 µm.

For the purpose of demonstrating the capability to pattern complex features, a second set of samples was produced with the following silver patterns such as: rings, concentric rings, concentric ring-shaped holes, dots, and i-beams. After lift-off and MacEtch, the corresponding reversal image of these patterns etched onto silicon, producing tubes Figure 19a), concentric circular walls (Figure 19b), concentric circular holes (Figure 19c), posts (Figure 19d), and i-beams (Figure 19e), respectively.

As discussed earlier, the most accepted diffusion model for MacEtch suggests that etching begins on the edge of an Au feature and progresses laterally and underneath the Au layer as opposed to going through the Au layer [78]. A rather non-intuitive result obtained and shown in Figure 19is that the areas of continuous gold catalyst (without patterns) etched uniformly onto silicon without catalyst folding or slower etch rates. Our main hypothesis to explain the occurence of uniform etching on continuous areas of Au film is the existance of sub-5nm cracks

in itself. These cracks are created when the evaporated Au layer is thinner than 10 nm. The evidence to sustain this hypothesis is depicted in Figure 19c-e where one can observe sub-5 nm thins of silicon emerging from the cracks and collapsed onto the substrate as a result of surface tension forces acting during the drying step in which samples underwent.

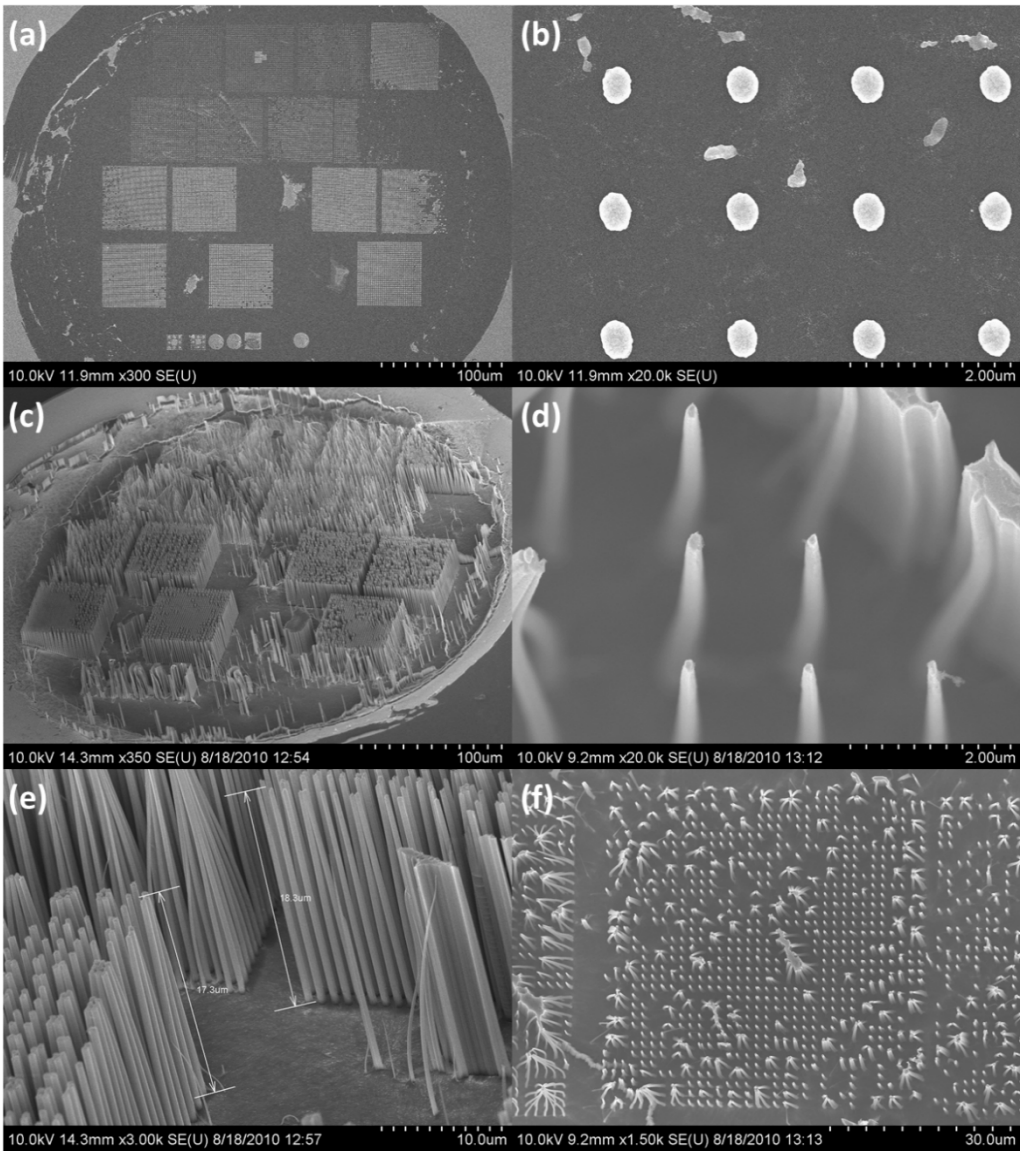

Figure 18: SEM images of arrays of silver dots made by S4 process (a-b) followed by its corresponding nanostructures after MacEtch (c-f). The etching throughout the entire sample was uniform even though the regions separating the arrays of dots was larger than 50 µm in some locations of the sample. The hypothesis is that small sub-5 nm cracks are present in the catalyst layer which facilitate diffusion through the cracks.

It is observable that the catalyst in the center of the tubes in Figure 19a as well as the catalyst rings in Figure 19b-c did not etch uniformly onto silicon. This phenomena is called catalyst folding and was studied extensively by Dr. Owen Hildreth and collaborators at Georgia Instittute of Technology [117, 118] and, more recently, by Dr. Carl V. Thompson at the Massachusetts Institute of Technology [119]. The origin of catalyst folding arises from different forces exerted in the Au layer as it is being etched. Dr. Hildreth argued that electrophoresis forces is one of the possible mechanisms for catalyst folding. While this understanding does not provide a solution, it helps to understand the limitations of the results obtained with the S4-MacEtch integration as it has failed to produce high-aspect ratio holes patterns or surpress catalyst folding.

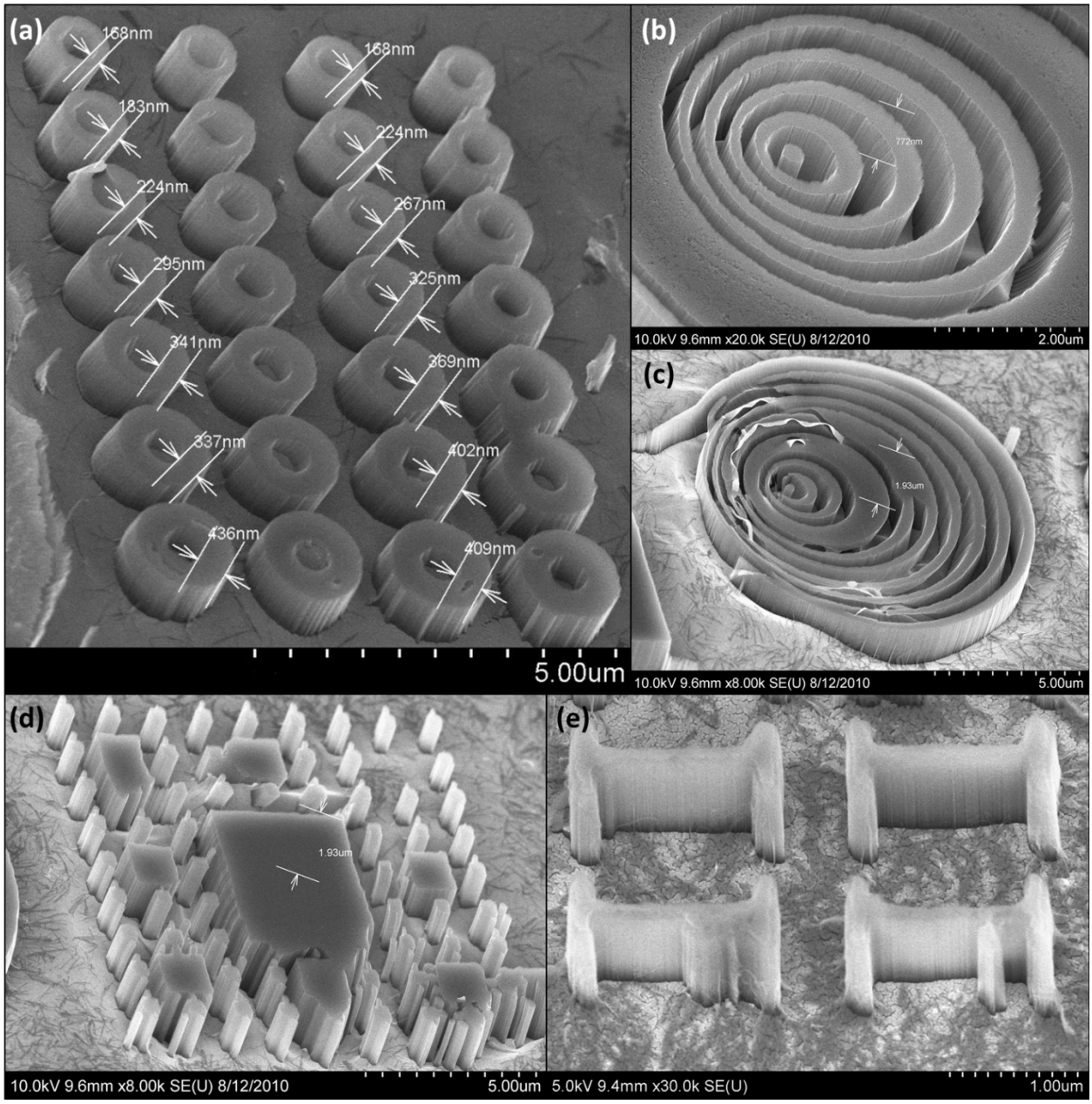

Figure 19: SEM images of nanostructures after S4 and MacEtch (a-e), demonstrating the versatility of producing complex patterns on silicon. In regions where the catalyst was thin and disconnected from the mesh, the catalyst folded onto itself producing

3.2 Nanoparticle Decoration Onto 1D Nanostructures Via Dewetting

In this section, we examine the decoration of SiNWs with Au-np by dewetting a uniformly sputtered ultra-thin film (i.e. less than 15 nm). Experimentally, we find that (a) the particle size increases with increasing annealing temperature, and (b) the contact angle is proportional to particle size and inversely proportional to annealing temperature. Computationally, a novel underlying mechanism for wetting of nanoparticles during dewetting is investigated: the formation of an amorphous layer of intermixed Au and Si atoms at the nanoparticle/substrate interface. This physical effect, observed in MD simulations, serves to increase the adhesion energy and explains the temperature-dependence of contact angle. Statistical data on particle contact angle was acquired as a function of annealing temperature and particle size using TEM imaging and image analysis, and agreed well with our MD model. Understanding how to control nanoparticle assembly onto SiNWs during dewetting may have impact in harvesting light-matter interactions to the benefit of technological applications aforementioned.

3.2.1 Experimental Methods

SiNWs were made according to the experimental procedure described in literature [35]. One large sample of SiNWs was sputtered with Au for 150 s at 40 % power in a Denton Desk V employing the all-angle stage rotation feature. Prior to selecting the deposition time, gold films were deposited onto SiNWs at 50s, 125s, 150s and 200s and inspected under SEM for continuity. At 150s and 200 s, the as-deposited film (i.e. no annealing) was continuous. Since sputtered metallic films deposited at room temperature (RT) are typically continuous at about 10 nm thickness, it is estimated that the deposition rate is approximately 0.8 Å/s and the film thickness

ranges from 5-15 nm. The sample was cleaved into smaller sizes and later immersed for 60 s in HF (48 wt. %) prior to annealing to remove the native oxide, rinsed with methanol, and immediately inserted into the annealing chamber while still wet. Samples were placed while still wet inside the annealing chamber and the chamber was pumped down to ~5E-7 torr. A vacuum level of approximately 10E-2 torr was achieved within 2 minutes of sample loading. Once this vacuum level was reached, the temperature was increased to the annealing temperature at a ramp rate of 200 °C/min and held there for 5 hours. Annealing time was selected to be an order of magnitude longer than previous studies [120, 121] on ultra-thin films (i.e. less than 15 nm thick) in order to allow it to fully dewet and reach thermodynamic equilibrium. Upon completion of annealing, the chamber was pumped down and the samples were immersed in methanol. This process occurred in under 1 minute. After annealing, the samples were stored in methanol to prevent oxidation of the Si substrate.

For TEM sample preparation, the SiNWs were removed from the methanol bath, scraped onto a lacy carbon grid using a clean razor blade, and immediately loaded into the TEM for characterization. Images were taken in bright-field TEM mode in a JEOL 3010 and using both bright field TEM and high angle annular dark field (HAADF) scanning (S)TEM imaging in a FEI Titan microscope, both operated at 300 kV. As each grid contained dozens of NW's to image, no tilting of the sample was necessary. Instead, the sample was translated in the x-y plane to locate nanoparticles protruding from the SiNWs, whose axis was approximately perpendicular to the electron beam direction, reducing any projection effects of the nanoparticle contact angles in the micrographs. It is important to note that the contact angle was measured in high-vacuum conditions (i.e. 8.8E-8 torr) which may alter the contact angle from its configuration in

atmospheric conditions. However, since the measurement is performed at RT, the nanoparticles are likely "frozen" in a meta-stable equilibrium due to lack of sufficient energy carry on the transition to a different configuration.

The contact angle and 2D projected particle area of gold droplets were calculated from TEM and STEM images using a freehand tool in ImageJ analysis package [122]. The particle's cross-section area was measured by approximating them as ellipses in the images. The lengths of the major ($2a$) and minor ($2b$) axes were measured for each ellipse and the projected area of the particle was calculated as $A = \pi ab$. The contact angle made by the particle was obtained by averaging the advancing and receding contact angle extracted on either side of the 2D particle image. To reduce the uncertainty produced by a tilted particle, both sides of the Au NP were manually fit with a triangle, and the contact angle was determined by the average value based on the law of cosines for the triangles fitted on either side of the particle. Within each image, a confidence is assigned to the particles based on clarity of the image, visibility of the individual particles, and ease of measurement of the contact angles for individual particles (i.e. nanoparticles perpendicular to the electron beam). Data were only collected from images that were assigned high confidence ratings. Further, very small particles (i.e. whose cross-section area is less than 25 nm^2) were not considered in the analysis, to avoid large error in measuring the angle of contact for such small droplets. Overall, 130 high confidence data points were collected and the data were binned according to the projected area of the particles, at each annealing temperature value. The variation of contact angle with the projected area of the particle was measured at three different temperatures: 323 K, 473 K and 673 K.

Lattice Considered	Results from MD Simulations		Computational results [123]		Experimental (or DFT) results [123]		Percentage error (%)	
	a (Å)	E (eV)	a (Å)	E (eV)	a (Å)	E (eV)	a (Å)	E (eV)
Pure Au (FCC)	4.092	-3.93	4.089	-3.93	4.089	-3.93	0.07	0
Pure Si (Diamond)	5.413	-4.334	5.431	-4.334	5.431	-4.630	0.3	6.3
Au-Si, B1 crystal lattice	5.362	-3.872	5.362	-3.873	5.28 (DFT)	-3.643 (DFT)	1.55	6.2
Au_3Si, $L1_2$ crystal lattice	4.194	-4.033	4.193	-4.035	4.145 (DFT)	-3.149 (DFT)	1.18	27

Table 1: Values for lattice structures of materials

Molecular Dynamics (MD) simulations were conducted to study the dependence of the contact angle on the annealing temperature and Au droplet size. In order to take into consideration the i) Au-Au pairwise interactions with non-directional bonding within the droplet, ii) Si-Si pairwise interactions with directional bonding within the substrate and, iii) Au-Si interactions with mixed metallic-covalent bonding at the interface of droplet and substrate, a unified angular-dependent embedded atom method (AEAM) interatomic potential was adopted [123]. The accuracy of the AEAM potential was validated by comparing the equilibrium lattice constant and cohesive energies of pure Au (with FCC lattice), Si (with diamond cubic lattice), and the cubic lattice superstructures of Au-Si system, including AuSi (with B1 lattice) and Au_3Si (with $L1_2$ lattice) with the corresponding values obtained from literature (see Table 1). The MD simulations were initialized with the Au droplet (initially as a sphere with diameters ranging from 30A to 400A) placed on top of a Si substrate constrained from any rigid body translation or rotation (as shown in Fig. 2a). A sensitivity analysis was conducted on the minimum size of the Si substrate, and no periodic boundary conditions were applied to the system. The atoms in the system were relaxed to find equilibrium using an NVT ensemble. For each droplet specific size, MD simulations were run for 100 ps at a fixed temperature; the simulations were repeated at

temperatures of 10K, 150K, 323K, 473K and 673K. The relaxed state of the Au-Si system was used to find the angle of contact between the droplet and substrate via MATLAB's image processing toolbox.

3.2.2 Particle Size Control

After annealing Au-coated SiNWs at 323, 473 and 673 K, the film fully dewetted into Au-np with diameters in the range of 6-70 nm (Figure 1). It was found that (a) increasing annealing temperature leads to an increase in particle diameter, and (b) the diameter distribution follows a Log-Normal distribution (Figure 1c). One possible explanation for the first observation is that there exists a competition in the kinetics of grain growth and grain boundary grooving during morphology evolution in the dewetting process [124]. At higher temperatures, grain growth can precede grain boundary grooving, allowing grains to merge before the break-down transition of the thin film. This effect leads to the formation of larger particles since thin-film grooving is energetically favored at grain boundaries [63]. At the same time, the second observation – of a Log-Normal distribution – is atypical since dewetting of metallic films onto atomically flat surfaces leads to a normal distribution of particle diameters [125, 35]. Two unique characteristics of the nanowire can affect the particle size distribution: the varying crystal orientation and surface roughness along its circumference. While particles may preferentially form at facets of the nanowire with the lowest energy configuration, dewetted nanoparticles were observed to form in nanoscopic grooves that spanned along the length of the nanowire (Figure 1b). SiNWs manufactured via metal-assisted chemical etching have such groove patterns along their lengths because of edge roughness originally present on the gold patterns used during etching [126]. As

the etching progresses, the edge roughness profile of the metal catalyst extends through the length of the wire during metal-assisted chemical etching, forming the grooves. These grooves serve as a template for self-assembling nanoparticles and, thus, potentially explain the occurrence of a Weibull distribution rather than a normal distribution.

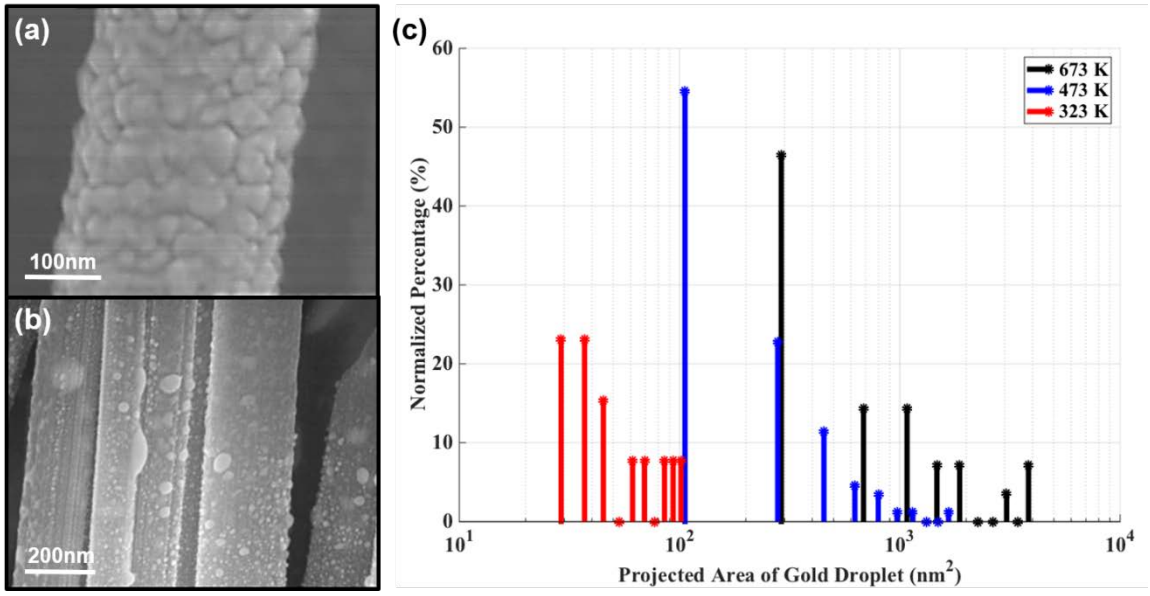

Figure 20: Dewetting characteristics of Au ultra-thin film onto SiNWs. Figures (a) and (b) are SEM images taken before and after dewetting, respectively, and highlight the assembly of nanoparticles throughout the length of the nanowires. Graph (c) shows the histograms of the particle size distribution along the nanowire as a function of temperature.

3.2.3 Contact Angle Control

In addition to particle size, the contact angle between dewetted particles and the nanowire surface was examined in detail. Annealed samples were imaged via TEM (Figure 2c-d) to resolve the contact angle as a function of particle size and annealing temperature. It was observed that the contact angle increases with (a) increasing particle size (a trend shown in Fig. 3a), and (b) decreasing temperature. The first observation can be explained based on the size-dependence of cohesive energy for nanoparticles whose size is in the range of 5-30 nm [127,

128]. As the particle size and the number of atoms in it decreases, the particle cohesive energy decreases [127, 128], leading to smaller contact angles (i.e. wetting). Another possible explanation might include the effect of line tension which has been argued to influence the size-dependence of the contact angle of nanoscale droplets [67, 129, 130, 131], but the presence of this effect is still debatable at this length scale and not previously investigated for materials below its melting temperature.

To understand the temperature dependence of the contact angle, it is important to consider mechanisms that govern nanoparticle shape evolution during dewetting. First, an increase in temperature activates kinetic processes (i.e. curvature-driven surface diffusion of Au atoms) that drive the film from a metastable (i.e. film) to an equilibrium configuration (i.e. particle) [63]. Simultaneously, a temperature increase can trigger diffusion across the Au-Si interface and, in theory, promote interatomic mixing even below T_E and form an amorphous layer at the Au-Si interface [69]. It is hypothesized that this layer exists, and its formation is accelerated as temperature increases, resulting in an increase in the adhesion energy and, consequently, a reduction in the contact angle. Thus, atomic mixing at the interface can explain the temperature dependence of the contact angle below T_E.

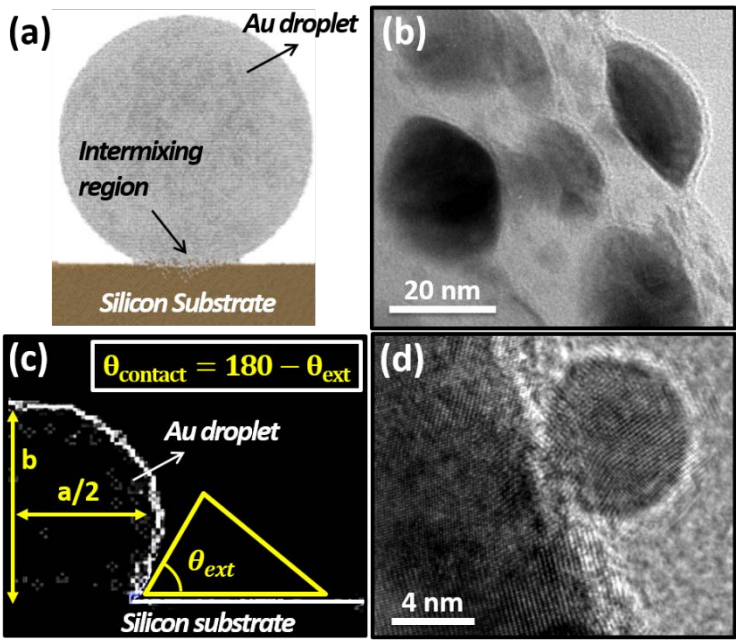

Figure 21: Molecular Dynamics simulation. Image (a) depicts MD simulation result of an Au-np on top of a silicon substrate. Images (b) and (d) are TEM images revealing the crystallinity, size and contact angle of Au-np onto SiNWs. Image (c) summarizes the image analysis method for obtaining particle projected area and contact angle. First, the particle shape is outlined via image processing of the TEM data. Next, "a" and "b" are measured and used to compute the projected area of the particle. Finally, θ_{ext} is measured by fitting a triangle near the triple line and contact angle is calculated according to formula inset.

In order to further investigate this hypothesis, MD simulations of Au particles onto Si were performed (Fig. 2a). It was observed that the contact angle (a) decreases with increasing annealing temperature for a given particle size, and (b) increases with increasing particle size. These trends qualitatively match experimental observations (shown in Fig. 3a) at temperatures below T_E. In Fig. 3a, each data point is the average of a set of contact angle measurements made on particles randomly dispersed on the SiNW surface. The large standard deviation in these sets is associated with variations in surface energy intrinsic to different crystallographic facets where particles are located. Single measurement error is 20 degrees. At temperatures above the Au-Si eutectic temperature (636 K), the experimental trend is not captured in the MD simulation (Figure 3). One of the possible reason for this disagreement is the lack of sufficient time to simulate larger particles which, ultimately, limit atom diffusion across the interface. By limiting

the simulation time, the simulation does not capture the formation of a superstructure above T_E which modifies the mechanism governing the contact angle [69]. The error in the prediction trend (above eutectic point) can also be partly attributed to the fact that there is an 8% deviation in eutectic temperature and 13% deviation in eutectic composition of Si predicted by AEAM potential [123], when compared with the experimental phase diagram.

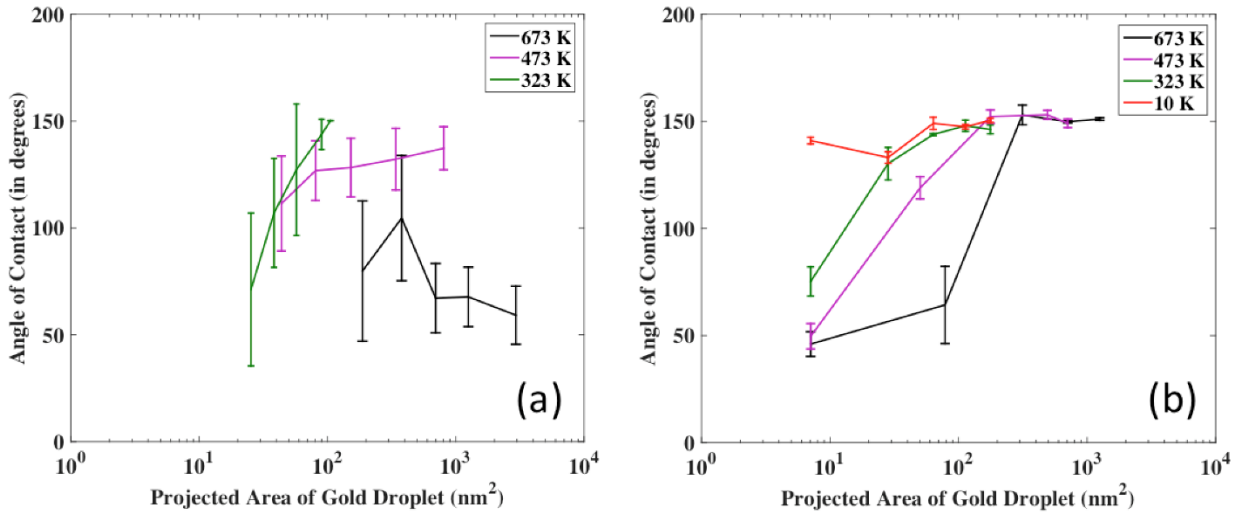

Figure 22: Contact-angle comparison between experimental and MD simulations results. Left graph (a) depicts experimental results while right graph (b) depicts computational results for contact angle as a function of particle size and temperature. The error of a single contact angle measurement is 20 degrees. Error bars in part (a) represent 1 standard deviation of a set of measurements made on particles sitting on a variety of crystal facets of SiNWs. Trends in temperature and particle size are captured well for temperatures below T_E.

The contact angle dependence on temperature can be related to changes in the adhesion energy due to atomic mixing at the interface. In the post-analysis of the simulation output, the Au-Si interface was examined using a radial distribution function to identify any possible coherence with particular lattice structures (Fig. 4). It was observed that an amorphous region formed between the Au particle and Si substrate as shown in Fig. 2b. A larger amorphous region was observed at higher temperatures, as expected, due to the increased diffusion kinetics. The amorphous intermixing regions led to larger distances between nearest neighbors in the Si

substrate and smaller distances between nearest neighbors in the Au-np. The intermixing region was indeed amorphous, as no obvious superstructure (B1 – AuSi or $L1_2$ – Au_3Si was observed in the simulations). Albeit at temperatures above the T_E, the average neighbor distance approached an AuSi superstructure, but in all cases, sufficient strain is present near the interface, thereby affecting the spacing of the lattice structure. For the crystalline constituents (Au - FCC and Si - DC) and superstructure (AuSi - B1), a defect-free lattice structure represents a minimum energy configuration. As the radial distribution function starts to deviate away from these lattice structures, additional disorder is introduced into the system resulting in an increase in the potential energy of the system. Therefore, as shown by the radial distribution functions, increased temperatures result in more intermixing and an increase in adhesion energy at the interface.

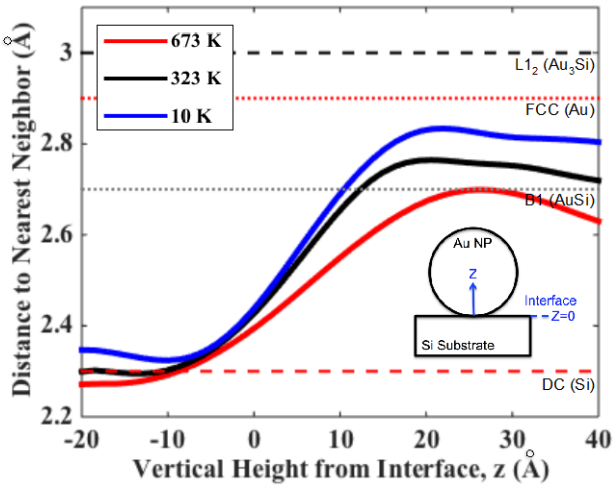

Figure 23: Radial distribution functions showing average distance to the nearest neighbor as a function of vertical height away from the interface (Z=0 is at the Au-Si interface) and annealing temperature. Equilibrium nearest neighbor distances for different materials are included for reference.

3.3 Chapter Summary

Self-assembly of gold nanoparticles onto high-aspect ratio silicon nanowires has been demonstrated via thin-film dewetting. The resulting morphology of dewetted particles (i.e. size and contact angle) was characterized via TEM imagining. Control over particle size was accomplished by varying the annealing profile, namely the set-point temperature. Nanoscopic grooves that span the length of the wires serve as a template for dewetting and modify the particle size distribution. Further, the contact angle of gold nanoparticles was determined experimentally as a function of annealing temperature and particle size. It is hypothesized that the formation of an amorphous AuSi layer regulates the temperature dependence of the contact angle. MD simulations were performed to examine this hypothesis. It was found that the simulation agrees with experimental data qualitatively below T_E. This correlation between experiment and simulation is attributed to the formation of an amorphous Au-Si layer at the interface that increases the adhesion energy and, thus, explains the contact angle dependence on temperature.

Chapter 4. Porous Silicon Patterning Via Electrochemical Imprinting

Two-dimensional microscale patterning of porous silicon (p-Si) offers many opportunities for exploiting its optical properties thru on-chip and heterogeneous integration. Applications in optoelectronics [15, 16], photonics [17], micro-thermal systems [132], lab on a chip [133], biodegradable materials [18, 19], in-vivo bio-imagining and drug-delivery [20, 21], and biosensing [22, 134] are derived from such integration. However, micro- and nano patterning of p-Si has remained a challenge due to the inability of standard microfabrication processes (e.g. photolithography, wet and dry etching) to effectively pattern porous silicon [135, 136, 137]. In this chapter, we demonstrate a low-cost, low-stress, ambient and high-throughput electrochemical nanoimprint approach to patterning smooth 3D curvilinear p-Si surfaces in a single imprinting operation. As a demonstration of this process, sinusoidal and parabolic surfaces with potential uses as diffraction gratings and concentrators are fabricated to demonstrate potential on-chip micro optical components.

Traditional approaches to patterning Si do not extend to p-Si because of the permeability and reactivity of the latter. During photolithography and micromachining, photoresist, developers and etchants infiltrate the pores, leading to contamination of the substrate, poor sidewall control and over-etching and, in general, poor fidelity of pattern transfer [135, 138]. Cost-effective wet etching processes such as KOH cannot selectively etch porous silicon since multiple crystal facets are exposed. Recipes for dry etching methods must be specifically tailored to a particular pore morphology of the p-Si being etched and high-aspect ratio features are seldom reported [135]. To circumvent these issues, microcontact printing (MP) [139], and other

methods described in section 2.2.2.1 were invented. The MP method was specifically designed for porous silicon and it uses a stamp that blocks diffusion of reactants during anodization of the silicon surface. As a result, it offers few degrees of freedom for 3D patterning and, thus, is limited to fabricating shallow corrugated patterns.

Additionally, it is often desirable to avoid photolithography and deep reactive ion etching (DRIE) to reduce complexity and cost of manufacturing p-Si. Metal-assisted chemical etching (MACE) is one alternative directional wet etching method for semiconductors [140, 141, 142]. Unlike its counterparts, it can "cut through" all crystal planes selectively [143], turning it into a good candidate for the development of an imprinting process. In the case of patterning silicon, it has been reported to produce high aspect-ratio (>100) features [144] with sub-10 nm resolution [145] and tunable sidewall profile with taper ranging from 0-13 degrees [35]. A large portion of MACE research focuses on understanding defect generation, namely pores that are created in the substrate, via fundamental studies [146, 147, 148, 149, 150, 151]. Moreover, while p-Si patterning can be obtained via MACE during the patterning process, the range of pore morphologies is limited, often not uniform and dependent upon the doping concentration and ratio of oxidizing to reducing species [152]. From research on the fundamentals of MACE, it is now understood that there is a balance between *(a) charge transfer (CT) kinetics at the catalyst-Si interface*, and (b) the rate of diffusion of reactants and products towards or away from that same interface. The ratio of these rates governs the relative rate of anisotropic etching to porosity generation [152, 153]. While the rate of electron-hole injection can be controlled by

tuning the concentration of the reducing agent, the diffusion can be promoted in various ways: (a) adding pores/cracks to catalyst thin-film [154], (b) reducing the length of the diffusion pathways (e.g. small widths of catalyst patterns) [153], and (c) increasing porosity of substrate. In fact, MACE of low-doped silicon can be said to be *stable* in the sense that increasing CT kinetics leads to increased porosity on the substrate (directly underneath the catalyst), promoting diffusion of Si-etching reactants and decreasing the rate of porosity generation.

From a process standpoint, there have been several reported efforts to improve the scalability of MACE as a manufacturing method, and to extend its capability to control the catalyst motion in three dimensions. On the one hand, thin-film based MACE still relies on 2D templating techniques to pattern the catalyst - such as photolithography [153], e-beam lithography [143], interference lithography [155], thin-film dewetting [35], nanosphere lithography [156], and block-copolymer lithography [157]. Since the catalyst cannot be reused, a new noble metal thin-film catalyst must be patterned for each new sample. This characteristic adds to the processing complexity, generates waste, and makes MACE's cost and scalability a function of other processes. Furthermore, the lithographic patterning must be compatible with p-Si which may lead to the aforementioned challenges. While there has been reported success in the control the catalyst etch direction to achieve 3D features via magnetic-assisted MACE [158, 159] and engineering the catalyst motion [160, 143, 161, 162], these approaches have limited control over the span of 3D features it can produce and have not been demonstrated to have high repeatability and spatial uniformity.

In this chapter, we seek to address the aforementioned issues by the development of a high-throughput, electrochemical imprint process called “Mac-Imprint” that uses MACE for patterning p-Si. Like current formats of implementation of MACE, it is capable of centimeter-scale parallel patterning with sub-20nm nanometer resolution, however, unlike them, it avoids need for lithographic patterning of the metal catalyst for each substrate to be patterned by using a reusable imprinting stamp. Further, unlike reported purely mechanical imprinting processes for p-Si [103, 102], it does so with minimal mechanical forces and no resulting plastic deformation or residual stresses. At the core of this patterning technique lies the use of a noble metal-coated stamp immersed in HF and H_2O_2 solution and brought in contact with a Si substrate to selectively induce etching of p-Si at the contact interfaces. The 3D pattern transfer fidelity between stamp and substrate is compared across different thicknesses of the porous layer on the silicon substrate. It is found that, in the case when there is no porous layer on the substrate (i.e., for etching single crystal silicon), the shape of the stamp is not transferred into the substrate with any discernable fidelity. Instead, etching of the substrate is observed at the edges of the contact interface. However, the high-pattern transfer fidelity observed for substrates with porous layers strongly suggests that the substrate porosity is essential to allow the diffusion of reactants and reaction products to and away from the contact interface. Finally, it is shown that the etch rate is limited by the local mass-transport and depletion of the reactants in the vicinity of the contact interface between the stamp and substrate. The developed p-Si direct chemical imprinting technique is shown to be capable of producing curvilinear features with mirror quality finish, including microscale sinusoidal gratings, and parabolic surfaces. Additionally, new capabilities are introduced such as catalyst reuse with sequential-stamping configurations. The developed

imprint process skips the need for photolithography and dry etching methods, and operates in ambient conditions. Such characteristics may facilitate the commercialization of novel p-Si based technologies.

4.1 Experimental Section

The subsections below describe the experimental work on (1) stamp and (2) substrate fabrication (i.e. porous silicon), (3) imprinting cycle, (4) imprinted morphology analysis, (5) sinusoidal-wave imprinting set-up, and (6) the characterization of optical concentrators built with imprinting.

4.1.1 Stamp preparation

Stamps were manufactured in two different methods: the first uses photolithography while the second uses a micromachined silicon chip. The first method starts by spinning a 3 µm thick layer of AZ1518 photoresist (PR) supplied by MicroChemicals onto a 4 inch (100) Silicon wafer. All wafers had resistivity in the range of 1-10 ohm-cm unless otherwise noted in the paper. This first layer was hard baked at 150 °C for 40 min and then a second layer was patterned by lithography and also cured at 150 °C for 1 hr. This curing is performed to get the patterned PR layer to reflow. Subsequent observations and measurements confirm that the reflow results in a parabolic cross-section of features in this layer. A variety of patterns were manufactured using different photolithography masks. Gold (100nm) with a chrome adhesion layer (10 nm) is sputtered onto the PR patterns.

In the second approach, arrays of lines and dots were fabricated onto silicon wafers using photolithography and subsequently etched with DRIE. A layer of PR (SPR 220^{TM} – 4.5, supplied by MicroChem, Inc.) was spun, masked, exposed, and developed according to the manufacturer's specifications. After forming arrays of 10 µm wide line and dot patterns, the PR was hard baked at 110 °C for 2 min and etched in DRIE to generate negative sidewalls to a final depth of 30 µm. Then, the photoresist was removed in acetone, cleaned with an O_2 descuum process at 200 W for 5min. The sample was immersed in a hydrofluoric acid bath for 2 min to remove the native oxide, rinsed with methanol, dried and immediately transferred to vacuum to minimize growth of the native oxide. A thin-film of chrome (200 nm) and gold (50 nm) was sputtered onto the sample to protect the silicon substrate and form the catalyst. Wafers patterned with these two methods were cleaved into 1x1 cm chips and mounted to a Teflon® holder using Chemtronics' CircuitWorks® conductive epoxy before stamping.

4.1.2 Preparing Porous Silicon Substrates

Silicon substrates (1-10 ohm-cm) were cut to size (about 1 in^2) to fit into an electrochemical cell with a backing electrode. Since large-area imprinting is being performed, it is necessary to have the enough etchant in the vicinity of the reaction. Therefore, square mesas are patterned on these substrates using lithography followed by either a KOH etch or DRIE. The mesas had a width of 400 µm and a period of 900 µm. Etching to different depths (by changing the etch time) produces mesas of different height. All results of this paper were obtained with mesa heights of 60 µm unless otherwise noted. This is used to vary the volume of the etching solution available for imprinting features on each mesa.

The back of the substrates were coated with Nickel and annealed at 320 °C in a rapid thermal annealing chamber that focuses an infrared light source on the sample (model SSA-P610C, manufactured by ULVAC-RIKO, Inc.) in N_2 environment for 3 min to form an ohmic contact. The cell was filled with HF (48% wt. % in water) and a cylindrical platinum electrode was inserted from the top and remained 5 mm above the substrate. Porous silicon was produced at a current density of 135 mA/cm^2 for 120 s. This results in a mesoporous (pore size 1-10 nm) silicon layer with of thickness 20 µm on the surface of the substrate.

4.1.3 Chemical Imprinting Cycle

The substrate was immersed in a HF-H_2O_2 solution, ρ, of 90-98% as defined in literature [152]. The stamp, mounted to a Teflon holder Figure 24, is brought into contact with the substrate using a servo-controlled motion state with a load-cell until a mechanical load of 4-10 lbf is developed (see Figure 24). The two are held together for a prescribed amount of time at which point the stamp is withdrawn and the imprinting/etching solution is removed. The substrate is immediately rinsed in water for 3 min and air dried for several hours before being analyzed.

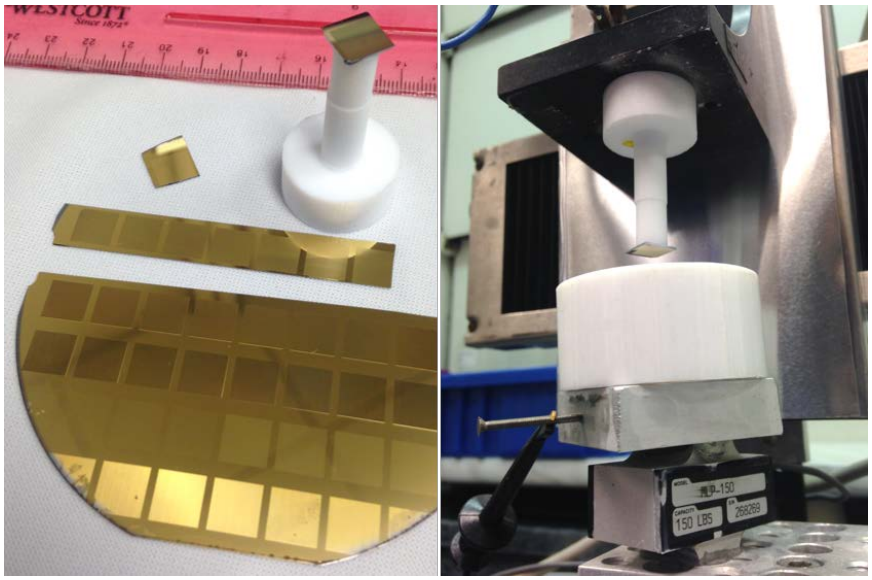

Figure 24: Experimental set-up for electrochemical imprinting showing (left) cleaved stamps cleaved and mounted into a Teflon folder and (right) stamp holder installed in a motion-controlled stage as it is inserted into the electrochemical cell for imprinting.

4.1.4 Sample Analysis

The dried imprinted samples are analyzed using an Atomic Force Microscope (AFM). The profile of the surface of the substrate is compared to that of the stamp. Given that the porous silicon substrates take the shape of the stamp which, for all of our experiments had a parabolic shape with a premeasured focus, optical images of the surfaces are sufficient to get a rough estimate of the volume of porous silicon removed. The optical images are analyzed to extract the width of the imprinted patterns. By assuming spatial uniformity of the focus of the parabolic cylinders on the stamp, the volume of porous silicon removed is estimated.

4.1.5 Fabrication of Sinusoidal Surfaces

A polyethelyne holographic film was obtained from Edmund Optics, Inc. (part no. 40-267) with a nearly sinusoidal pattern whose pitch was 1 μm and amplitude was 250 nm, respectively.

The film was sliced into 8 mm x 30 mm pieces, cleaned with isopropyl alcohol and sputter coated with a thin-film of chromium and gold whose thickness was 10 nm and 100 nm, respectively. The plastic film was wrapped around a Teflon cylinder whose diameter was 1 cm and held in place with Kapton® tape Figure 25. The cylinder was then mounted to the stamping stage and pressed against the porous silicon substrate with a constant load of 0.5 lbf for 2 min. The topology of the surfaces of the stamp and substrate were measured in an AFM with a super sharp tip (with a 3 nm radius) at the exact same complementary locations. The 3D point data of the stamp was plane leveled, cropped and inverted, and overlaid with the also plane leveled substrate data such that small complementary defects on both surfaces were aligned. The RMS of the difference between the overlaid data sets was measured using a Mathematica® code.

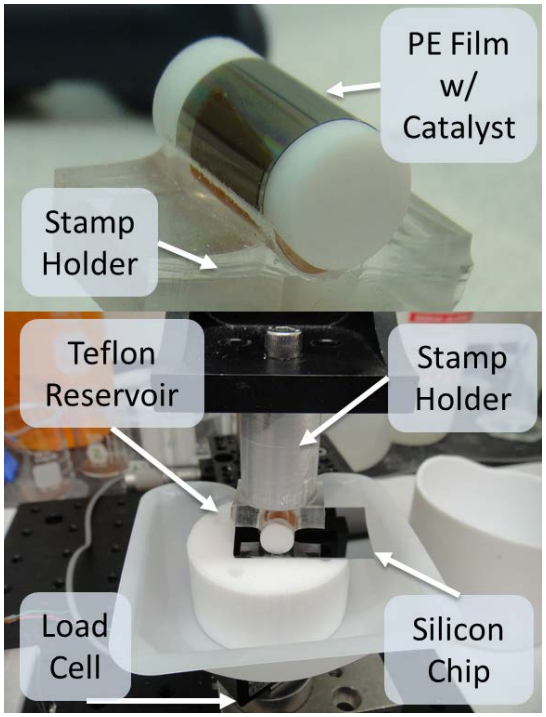

Figure 25: Experimental set-up for electrochemically imprinting silicon with plastic gratings mounted to a roller stamp

4.1.6 Microconcentrator Optical Characterization

Two samples, each containing parabolic cylinders or paraboloids, were mounted into a Zeiss 710 Multiphoton Confocal Microscope and illuminated with a continuous wave 405 nm laser. The imaging was done using the reflection mode of the system where the light is reflected 90° at the dichroic mirror (MBS 405) and the same light reflected off of the sample was detected in air with a Zeiss 10x EC Plan-Neofluar objective with a numerical aperture of 0.3. Since the experiment is not photon-limiting as in fluorescence, the pinhole diameter was reduced to 0.2 Airy units (5 µm), to achieve the highest spatial resolution in a confocal system [163] which was calculated to be 715 nm (lateral) and 5.6 µm (axial). A stack of 68 optical sections through Z dimension (out-of-plane) in 1 µm increments were obtained to reveal the focus point of the parabolic cylinder and paraboloid. The images were analyzed in Zeiss' Zen 2008 software.

4.2 Mass Transport and Chemical Storage

In an imprinting or stamping process, the objective is to transfer the shape of the reusable stamp into the substrate. As has been demonstrated by the large volume of literature on MACE, highly-localized etching of silicon is produced at the contact interface between the metal catalyst and silicon. Hence for imprinting, notwithstanding the changes in the geometry of the contact and reactant access to the interface between metal catalyst and silicon, one would expect similar localized etching of silicon to the contact interface, resulting in transfer of the shape of the stamp to the substrate since the underlying reaction mechanism remain unchanged. However, when imprinting directly onto a (non-porous) silicon substrate patterned with the mesas described earlier (to ensure local storage of reactants), a pattern of porous silicon develops directly beneath

and around the contact interface. Additionally, at the end of an etching cycle, the topography of the surface generated does not resemble that of the stamp (as shown in Figure 26a and Figure 27). Over-etching of the silicon around the edges of the contact interface leads to a 'double-dip' cross-section profile Figure 26a. These observations are consistent with the experimental findings and diffusion model by Geyer et al [17] that suggests that in the absence of sufficient diffusion pathways for reactants to reach the Si/Au contact interface, porous silicon formation around the edges of the contact interface is accelerated relative to the directional and localized etching of silicon. Given that the stamp is impervious to the etchants, as the etch progresses and a contact interface with sufficient lateral dimension (> 1 μm) develops, no pathways are left for diffusion to its center. We observe the same uneven etch profile from the edge to the center of the contact interface as observed in thin-film based MACE [153] along with the concomitant reduction in etch rate. Indeed, in all trials involving non-porous silicon, imprinting stopped at a

depth between 100 to 300 nm without achieving any fidelity between the etched profile and the stamp profile.

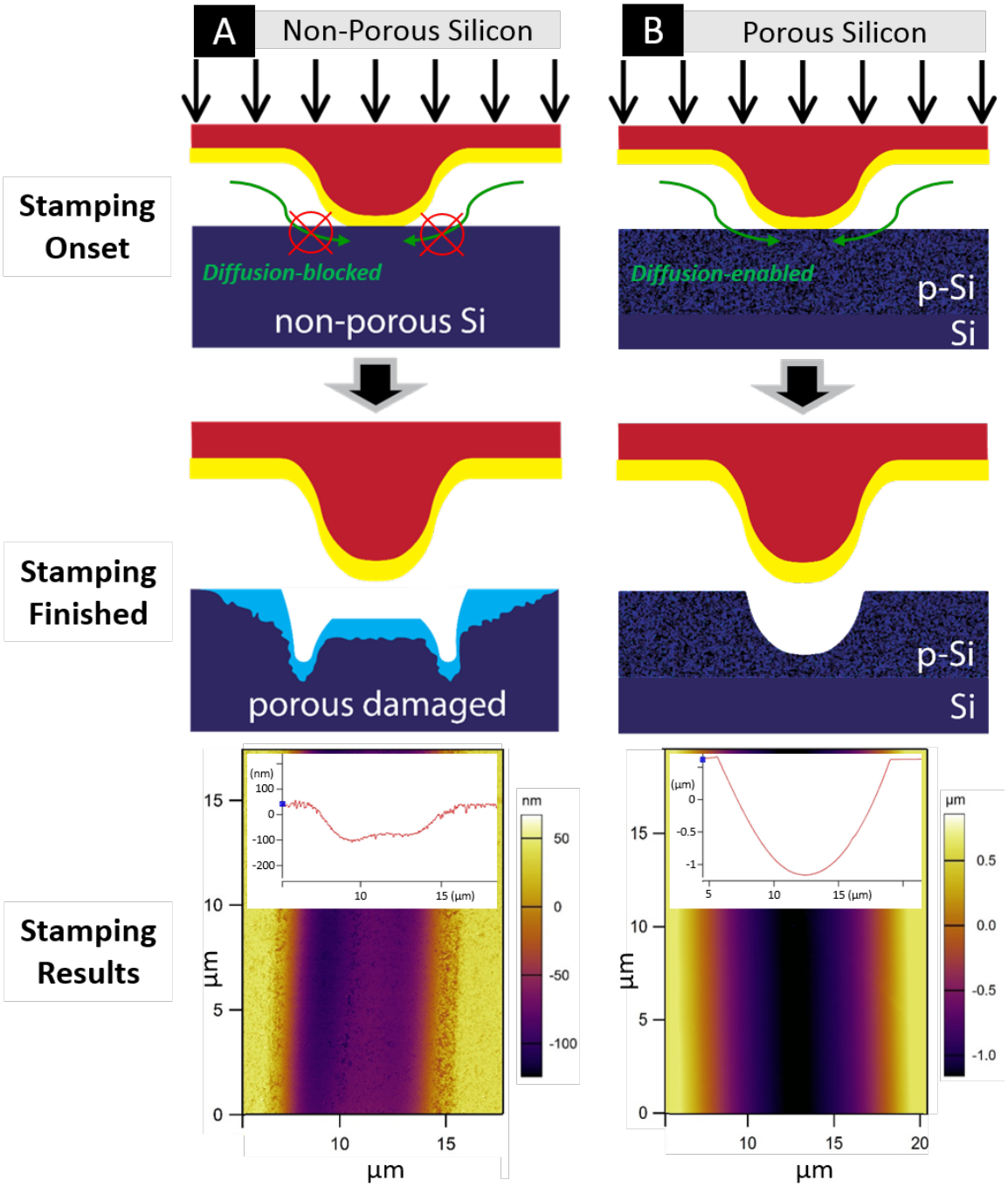

Figure 26: comparison of imprinting profile for porous vs. non-porous substrates. In part A, the schematics of a stamping operation onto a non-porous silicon wafer in which the substrates does not take the shape of the stamp and instead growth of porous silicon surrounding the catalyst-substrate interface in a "double-dip" pattern is shown (top and middle). In part B, the schematics of stamping operation into porous silicon in which the substrate takes the shape of the stamp is shown (top and middle). Finally, the bottom row depicts AFM scans of imprinted surfaces and corresponding cross-section profiles (insets) for non-porous silicon substrates (part A) and porous (part B) and, respectively.

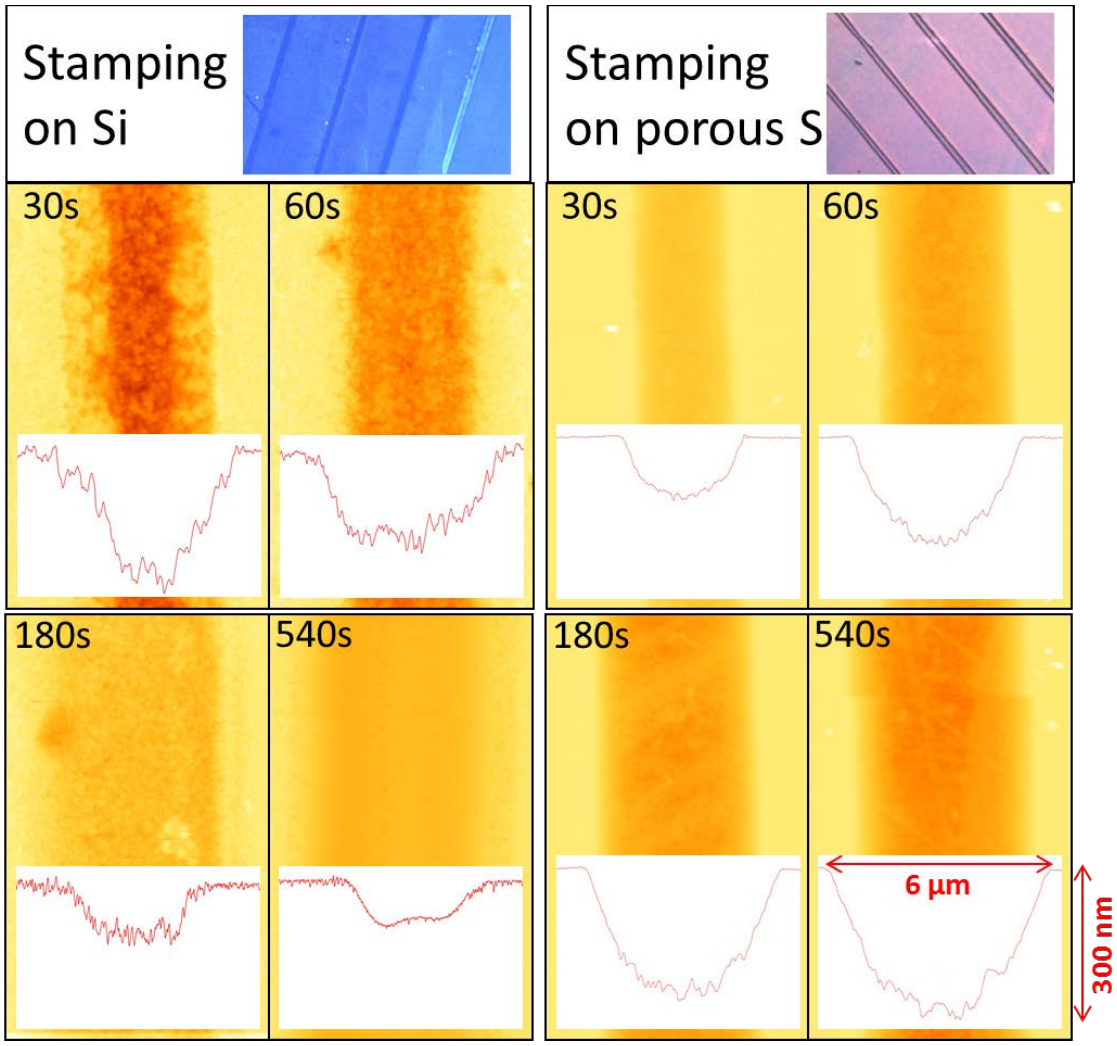

Figure 27: The evolution of the etch profile of substrate upon imprinting with a parabolic cylinder stamp is depicted for the case of etching silicon (left) and p-Si (right) for different times as labeled.

Additional data on the differences between imprinting porous silicon and non-porous silicon substrates was obtained. To contrast such difference, the two types of substrates were imprinted using the same stamp (parabolic cylinder) and stamping conditions of force, ρ-parameter and time. AFM profile of the imprinted non-porous substrate is shown for different etching cycles in the left half of Figure 27. The evolution of the profile in time does not resemble the shape of the stamp supporting the argument of mass-transport limitation in such cases as described in the paper. On the right half of this image, the imprinted shape has a parabolic shape

for short and long etches, highlighting the effect of pores in enabling the diffusion of reactants and products through its network of pores. In the case of non-porous silicon substrates, instead of the directional and selective imprinting of the features, a pattern of pores develops around the catalyst-stamp interface as depicted in the SEM images of Figure 28. The limited mass-transport leads to non-localized porosification of silicon and quickly depletes the supply of reactants limiting the depth of etched patterns to the 100-200 nm level.

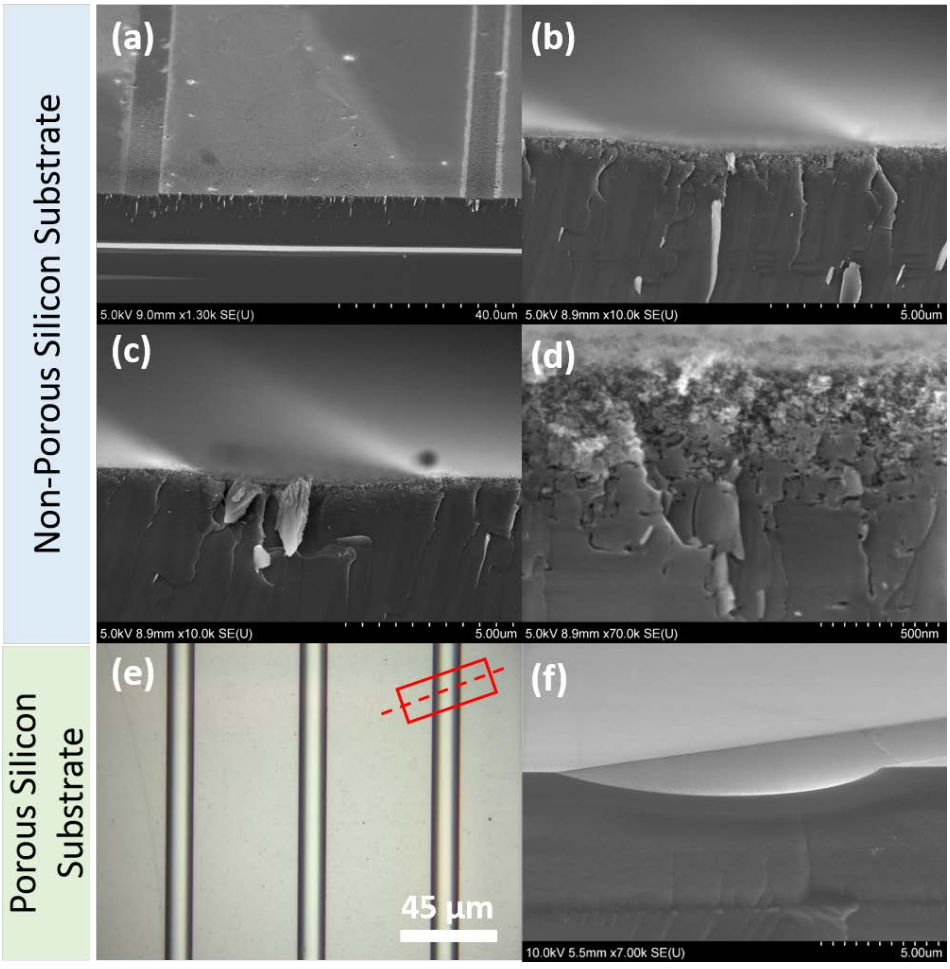

Figure 28: Images (a-d) depict SEM images of the cross-section of silicon substrates imprinted with parabolic cylinder shapes at different magnifications. These first four images reveal the preferred porosification beneath the stamp-substrate interface rather than the selective etching and imprinting of features with high pattern transfer fidelity. Additionally, image (e) depict a top down optical image of parabolic cylinders imprinted onto porous silicon and its corresponding cross-section (whose direction is highlighted in red).

Finally, the “double-dip” pattern obtained when stamping into non-porous silicon is shown in Figure 29. A ring with parabolic cross-section shape was used to imprint non-porous silicon. It is observed the accelerated etching around the outer edges of the contact interface. This results suggests the diffusion limitations imposed by the impervious stamp and substrate limiting the progression of the etching at the contact interface and rather in the surrounding domain.

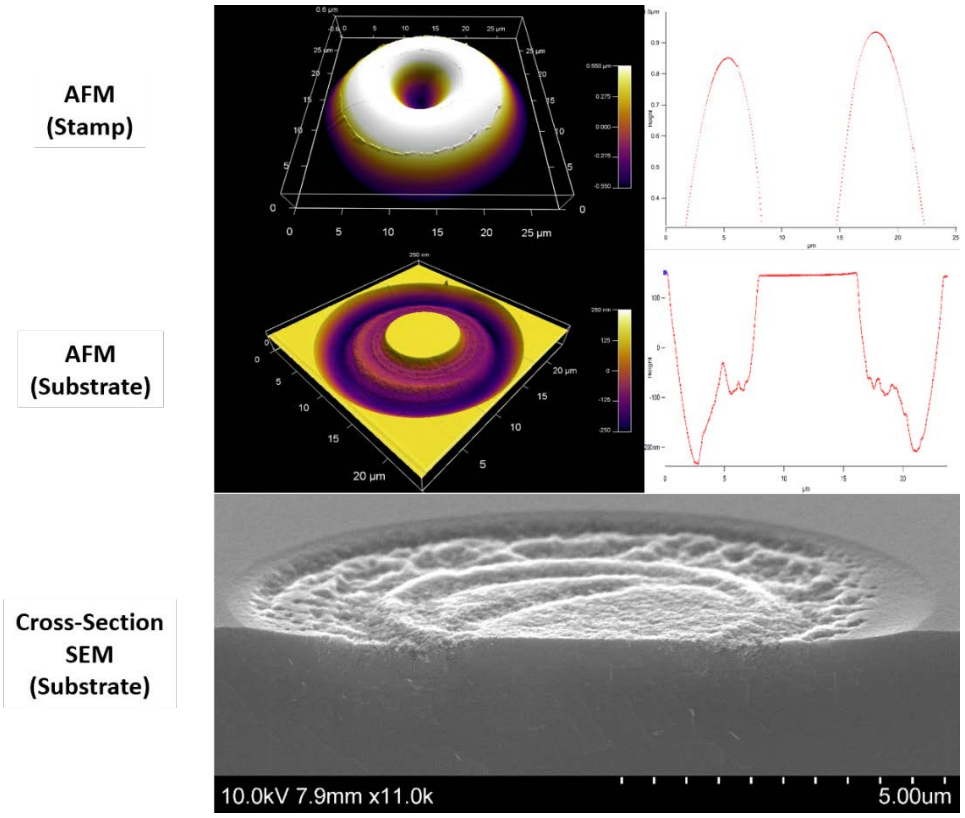

Figure 29: The top and middle rows depict AFM scans of the stamp and non-porous silicon substrate after stamping. On the left it is shown the AFM 3D profile and on the right the cross-section of the pattern. The profile is not transferred and rather an accelerated etching rate around the pattern develops forming what it is referred to a “double dip” pattern. In the bottom row, a representative SEM cross-section depicts the pore distribution near the edge.

Figure 26b shows a schematic of the process and the results of imprinting porous silicon. With a layer of porous silicon on the substrate, the process yielded consistent, high-fidelity

imprinting of the stamp geometry into the substrate. Besides faithful imprinting results, the volume of p-Si removed for a given etch time greatly increased and the process was observed to continue imprinting to depths of a few microns (limited only by the height of the features on our stamps). All process condition being the same in the two cases of imprinting on porous and non-porous silicon substrates, it can be inferred that the porous nature of the substrate facilitates the mass-transport of reactants and products to and from the contact interface, making it possible for the etching reaction to continue while remaining localized at the contact interface between the stamp and substrate. Without the porous domain the process not only stalls, but also fails to replicate the topography of the stamp on the substrate.

With a porous substrate, one can now think of the imprinting process as a transport-limited process with the reaction limited by the fact that the reactants and products have to diffuse through the pores to get to or from the reaction zone, as shown in Figure 30a. To characterize the kinetics of the process, the volume of porous silicon removed was measured as a function of etching time imprinting repeatedly for different lengths of time. Figure 30b shows

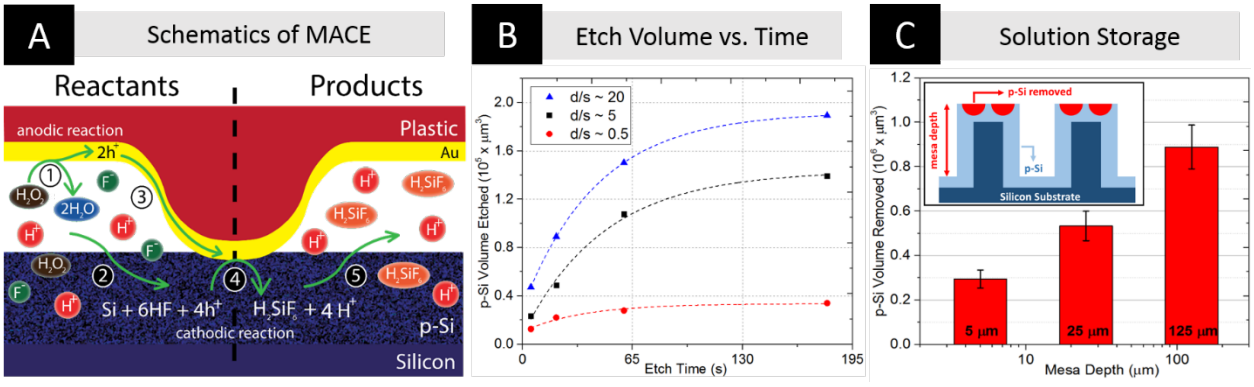

Figure 30: In part (a), the schematic highlights the (1) diffusion of hydrogen peroxide to the cathode and its reduction, (2) diffusion of hydrofluoric acid to the anode interface, (3) charge transport between the anode and cathode, (4) the oxidation reaction at the anode and (5) diffusion of products away from the anode. In part (b), volume of p-Si removed as a function of time shows the depletion and diffusion limited phenomena in imprinting (the dashed lines are exponentially decaying functions fitted to each data set). In part (c), the volume of porous silicon removed during a single stamping operation under the same etching conditions (time, force, and ratio of HF and H_2O_2) is plotted for 3 different volumes of solution confined between stamp and substrate.

the volume of p-Si removed as a function of time for three imprint depth to thickness of porous layer (d/s) ratios. For each d/s ratio, it can be observed that, unlike the conventional thin-film based MACE process, the volume of p-Si removed does not scale linearly with the etch time. Instead, it decreases exponentially as the imprinting process continues. At the onset, reactants trapped at the interface between stamp and substrate provide for a high material removal rate. However, these are quickly depleted, requiring additional reactants to diffuse from the surrounding solution located at a length scale of 20-200 μm away from the etching interface, and through the porous layer to replenish the reactants at the interface, thus slowing the imprinting rate. As the imprinting progresses, the diffusion length increases, thus producing smaller increments to the volume of p-Si removed with each additional time increment. Comparing across the three d/s curves, it is also found that the rate of material removal depends on the thickness of the porous silicon. For the case of d/s∼0.5, it is probable that the stamp encountered the solid silicon sub-surface during the process interval studied, resulting in the virtual stoppage of the imprinting process. The difference in the etch rates for the d/s∼5 and ∼20 cases suggests that the network of rich diffusion pathways below the interface zone play an important role in the transport phenomena associated with the process. Thicker porous layers increase the total amount of reactants present and extend the terminal etch depth.

The previous discussion suggests that the imprinting process is transport limited with the network of pores in the substrate serving to locally transport the reactants to, and the products from, the stamp-substrate interface so as to sustain the etch reaction and keep it localized. However, in an imprint process, one is typically interested in patterning over large areas (typically > 1 cm^2), which would require the network of pores to support the mass transport of the

reactants and the products over much longer length scales. To further understand if the local availability of reactants influences the process rates, the volume of solution confined in close proximity of the patterning interfaces was varied by changing the depth of the 'mesa' patterns in the substrate. Substrates were prepared by using a DRIE process to pattern square mesas (of 400 µm width) in a square grid (of 900 µm pitch) to depths: 5, 25, 125 µm. They were porosified at the same current density and time, forming a layer with uniform thickness (20 µm) about the mesa surface. This is done to ensure that the pore morphology and thickness are the same across the substrates, and, thus, are not a factor in determining the imprinting rates. Subsequently, the substrates were imprinted under the same time (180 s), ρ-parameter (96%) and force (4 lbf). The volume of material removed is shown in Figure 30c. It can be observed that the volume of p-Si removed scales linearly with the depth of the mesa pattern and, hence, the volume of reactants confined (and available locally) between stamp and substrate. Thus to implement a large-are, high-rate imprinting process, strategies for storing and confining sufficient reactants locally (used in this paper) or supplying them in close proximity to the features being imprinted must be developed so as to sustain the imprinting/etching reaction and permit it to progress at the desired rate.

4.3 Balance of Anodic and Cathodic Reaction Kinetics

In a typical MACE configuration that uses a thin-film metal catalyst, a number of factors dictate the morphology and spatial distribution of the pores produced during the etching process. These include: the doping level of the substrate [147, 146], width of the features of the metal catalyst [153], thickness and morphology of the metal film [153], ρ-parameter of the etching

solution [152] and the presence of organic co-solvents [35]. The ratio of the cathode area to the anode area is not, however, considered a factor thus far, because the process configuration is such that the entire bottom surface of the catalyst is in contact with the silicon surface through the entire etching process. Thus, with the top surface of the thin film being the cathode, the ratio of the cathode area to anode area remains constant at unity. In the imprinting configuration, depending on the stamp construction and geometry being imprinted, not only this ratio is much larger at the onset of etching, but it also reduces with time as the contact interface between the stamp and substrate evolves and increases during the imprinting process.

Since the rate of reduction of hydrogen peroxide scales with the area of the cathode and given the small area of the interface between stamp and substrate (that serves as the anode), it

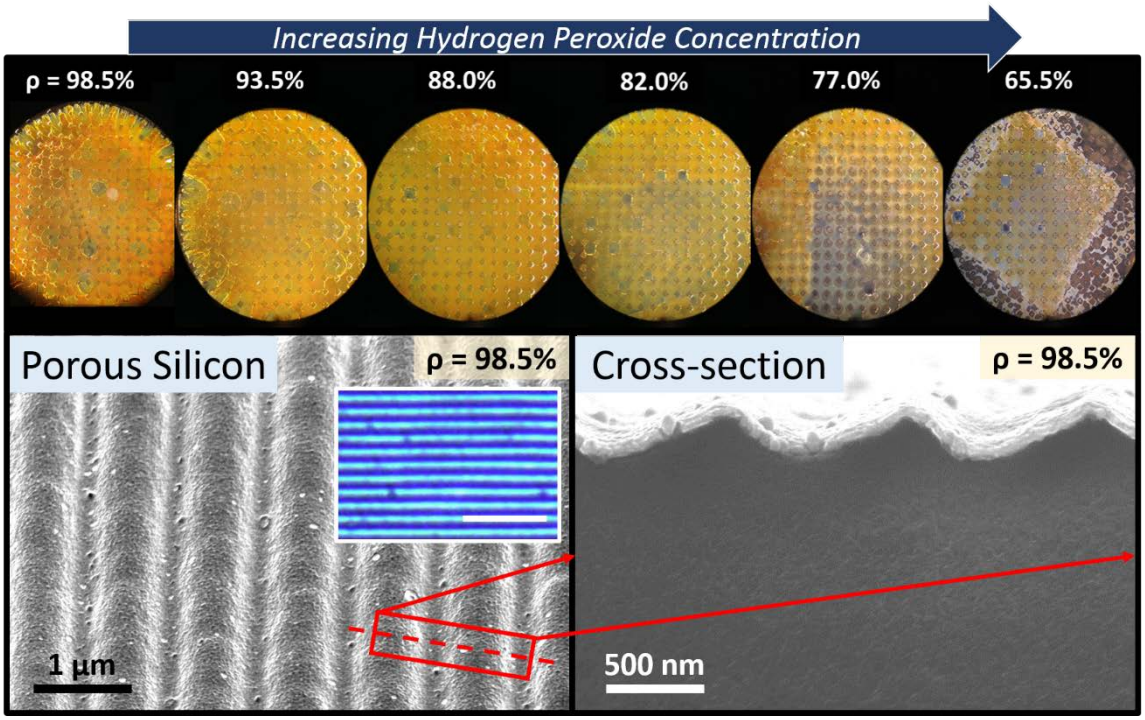

Figure 31: In the top row, optical view of mesas of porous silicon at 2.2x magnification after a stamping operation and as a function of the ρ-parameter (as labeled). For a reference of scale, the pitch between two mesas, seen in the image as small periodic dots, is 900 um. In the bottom row, an SEM of the 30˚ tilted (left) and cross-section (right) of sinusoidal patterns reveal its smoothness and the porous uniformity near the imprinted features. The Inset in the left image depicts an optical picture of the sinusoidal grating under angled illumination.

becomes difficult to localize the oxidation of silicon at ρ-parameter equal to 75-85% which is typically used in thin-film based MACE of low doped p-type silicon. Thus, the delocalization of etching reaction can lead to enlarging of the existing pores and non-specific etching of the silicon on the substrate, depending on the electrical fields developed, charge migration and availability of reactants. Thus, when designing stamps for this imprinting process, it becomes desirable to avoid large area ratios and, when unavoidable, compensate for it by increasing the ρ-parameter of the etching solution to reduce the rate of reduction of hydrogen peroxide.

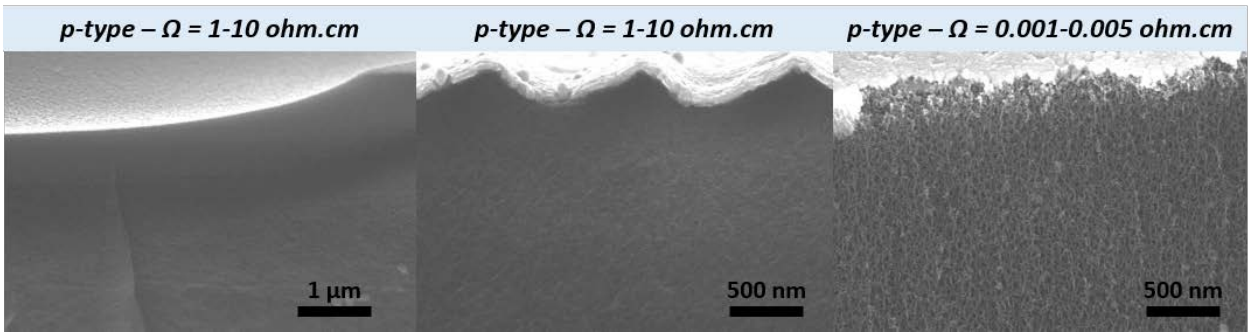

Figure 32: Pore size characterization. The left and center images depict the cross-section SEM of p-silicon while the right image depicts p+ substrates.

The effects of excessive hole generation can be examined by qualitatively studying the appearance of the porous silicon substrate before and after imprinting. Figure 31 shows substrates imprinted with etching solution with different ρ values. Examining the color appearance of the porous substrate before and after stamping, we do not observe any changes in the color of the porous substrate at high-ρ values (90-95%), but we see a dramatic darkening of the substrate when operating at low-ρ values (65-85%), or high volume fraction of hydrogen peroxide. The color change is attributed to widening of the pores and further porosification of the substrate. Further, in the high- ρ regime, scanning electron micrographs of the cross-section of the imprinted features confirm the uniform porosity surrounding them (Figure 31). This trend

is also observed in thin-film based MACE. However, in the case of imprinting with etching solutions having low-ρ values, the imprinted features in the p-Si also do not resemble those on the stamp and instead the surface is roughened (Figure 32).

4.4 Metrology and Process Characterization

For this imprinting process to be deployed as a practical micro- or nanofrabrication process, it is important to examine process characteristics such as resolution, accuracy, repeatability, defect density, and patterning speed. The former was determined using a soft

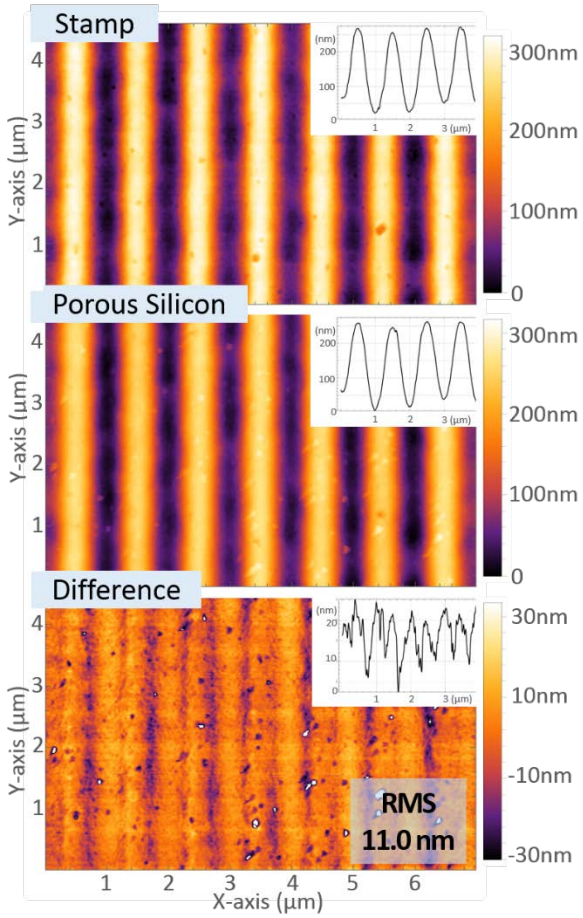

Figure 33: Determination of the resolution of MACE-imprinting with a near-sinusoidal test stamp. In part (a), the images depict AFM scans of the stamp (top) and substrate (middle) at the complementary location, and the difference between them after plane leveling (bottom), noting that the stamp scan (top) was inverted such that its peaks and valleys depicted correspond exactly to the same location on the substrate (middle) image. The insets show the cross-section profile of its corresponding AFM scan and the RMS value of the bottom surface plot is highlighted.

polyethelyne linear holographic film with a nearly linear sinusoidal pattern whose pitch and amplitude were 1000 and 250 nm, respectively. The film was cleaned and coated with the catalyst as described in the experimental section and used for imprinting. Figure 33a shows images of precisely complementary locations on the stamp and substrate with a high-resolution AFM. The 3D point data of both stamp and substrate was leveled with only a plane, the point set corresponding to the stamp was overlaid on the point set for the substrate and subtracted from it to produce the third image in Figure 33a. It was found that the RMS of the difference in heights between complementary points in the two images was 11 nm (Figure 33a). If we take the resolution of the process to be two times this RMS value, then it is consistent with the best resolution results achieved with thin-film based MACE research [145]. Other process characteristics are only discussed qualitatively. Accuracy, defect density and precision are affected by the degradation of the polymeric stamp which becomes evident after 10-15 uses due to delamination of the catalyst thin-film from the stamp. Small grains of gold fall into the sample after each stamping operation and large portions may peel off typically after the 10^{th} imprinting cycle (Figure 33b) depending upon the loading condition. Finally, uniformity of etch depth is largely dependent upon alignment and flatness of the stamp. This might be greatly improved with the development of a step-and-repeat automated system.

To assess the versatility of the imprinting process, stamps were made using the fabrication process described in the experimental section for imprinting parabolic cylinders, paraboloids and straight wall channels in porous silicon. Figure 34 shows optical images of the stamp and imprinted porous substrate as well as AFM profile scans of the imprinted features and cross-section graphs. During imprinting of the straight wall channel, a DRIE micromachined silicon

trench was used as the stamp instead of the polymeric stamp previously used. A thicker film of Cr (200nm) was sputtered onto the stamp as both an adhesion layer and protection layer for the silicon stamp. While the imprinting had a high pattern fidelity in some areas of the porous substrate, stamp degradation due to catalyst being undercut and peeling off onto the substrate surface was observed after the first stamping operation. Au particles peeled from the stamp resulted in roughening of the surfaces of the imprinted substrate.

Additionally, imprinting was demonstrated in porous silicon substrates with two distinct doping levels (0.001-0.005 ohm.cm and 1-10 ohm.cm) porosified under the same current density (135 mA/cm^2) and time (120 seconds). In the literature of porous silicon fabrication, there is a myriad of methods for controlling the pore morphology [135]. Among all of these methods, it is inherent to the porousification process the creation of pore pathways connected to the p-Si surface. However, not all of them generate a percolated network of pores that allow for lateral diffusion. In fact, some porosification techniques create pores that are directional and isolated from each other [138]. While Figure 34 shows successful imprinting into a limited set of p-Si

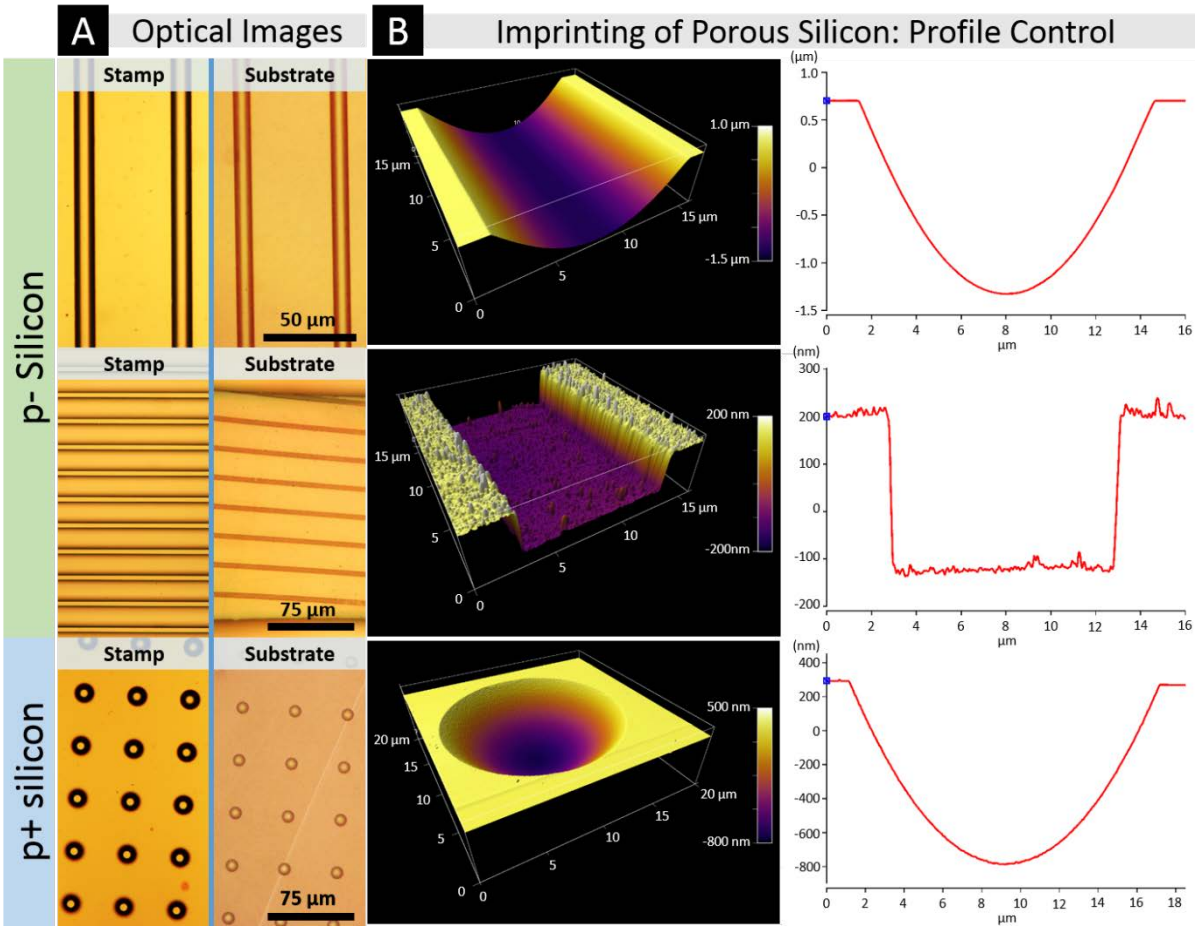

Figure 34: In part (a), optical top-down images of the stamp before imprinting and the substrate afterwards for different 3D geometries: parabolic cylinder (top), trenches with straight sidewalls (middle), and paraboloids (bottom). In part (b), 3D plot of AFM scans of the corresponding porous silicon surfaces are shown. The first two rows of images depict patterning of p- (1-10 ohm.cm) while the third row dipicts p+ (0.001-0.005 ohm.cm) p-Si substrates.

morphologies, MACE has been demonstrated to anisotropically etch silicon wafers of all orientations, doping types and levels [140]. Thus, based on the diffusion arguments aforementioned, it is expected that, as long as the substrate has a network of percolated pores that allows for diffusion to take place laterally (perpendicular to the motion of the stamp), this technique can be extended to a wide range of morphologies and doping type of p-Si.

4.5 High-Quality Reflective Micro-Concentrators

The advantages of low roughness (mirror finish) surfaces with high fidelity shapes can be best demonstrated by constructing a microscale optical concentrator whose conformance to a parabolic shape directly defines its quality. Stamps for imprinting parabolic cylinders and paraboloids can be manufactured by reflowing photoresist patterned into lines or dots, respectively. Such a stamp was used to pattern porous silicon using the method described in this paper. The surfaces produced are coated with a 30 nm layer of a reflective material (AuPd) to form a microconcentrator (Figure 35a). Figure 35 shows AFM scans of the surface profile of these geometries replicated onto p-Si. Using least squares, each profile is fit to a parabolic cylinder and paraboloid with a focus of 5.8 µm and 15.7 µm, respectively, and an RMS error of 18 nm and 23 nm, respectively. Next, the microconcentrators were illuminated with a collimated laser beam at 405 nm and the reflected light off of the microconcentrators was imaged at different focal planes through the Z dimension (out-of-plane) utilizing the inherent optical sectioning property of the de-scanned reflected light through a tight (0.2 AU) pinhole with a multi-photon confocal microscope (Figure 35b). Diffraction limited optics together with shape variations due to aberrations from a perfect parabolic profile lead to spatial widening of the full-width-half-

maximum (FWHM) of the Gaussian-shaped intensity profile. The measured focal plane was identified to be 10 µm and 26 µm above the surface and the FWHM of its focal spot measured to be 633 nm and 800 nm (Figure 35b). These measurements are very close to the theoretical lateral resolution of the confocal microscope under the set-up which was calculated to be 715 nm [163]. The difference between the focus of the parabolic shape and the position of the focus measured in the confocal microscope setup is attributed to the numerical aperture (0.3) of the lens used during imaging which deviates from the normal incidence assumption. The ability to focus light to a spot whose lateral dimension is only about 1.5 times its wavelength without significantly distorting the electromagnetic wave front suggests high quality of the shapes produced by the nanoimprinting approach.

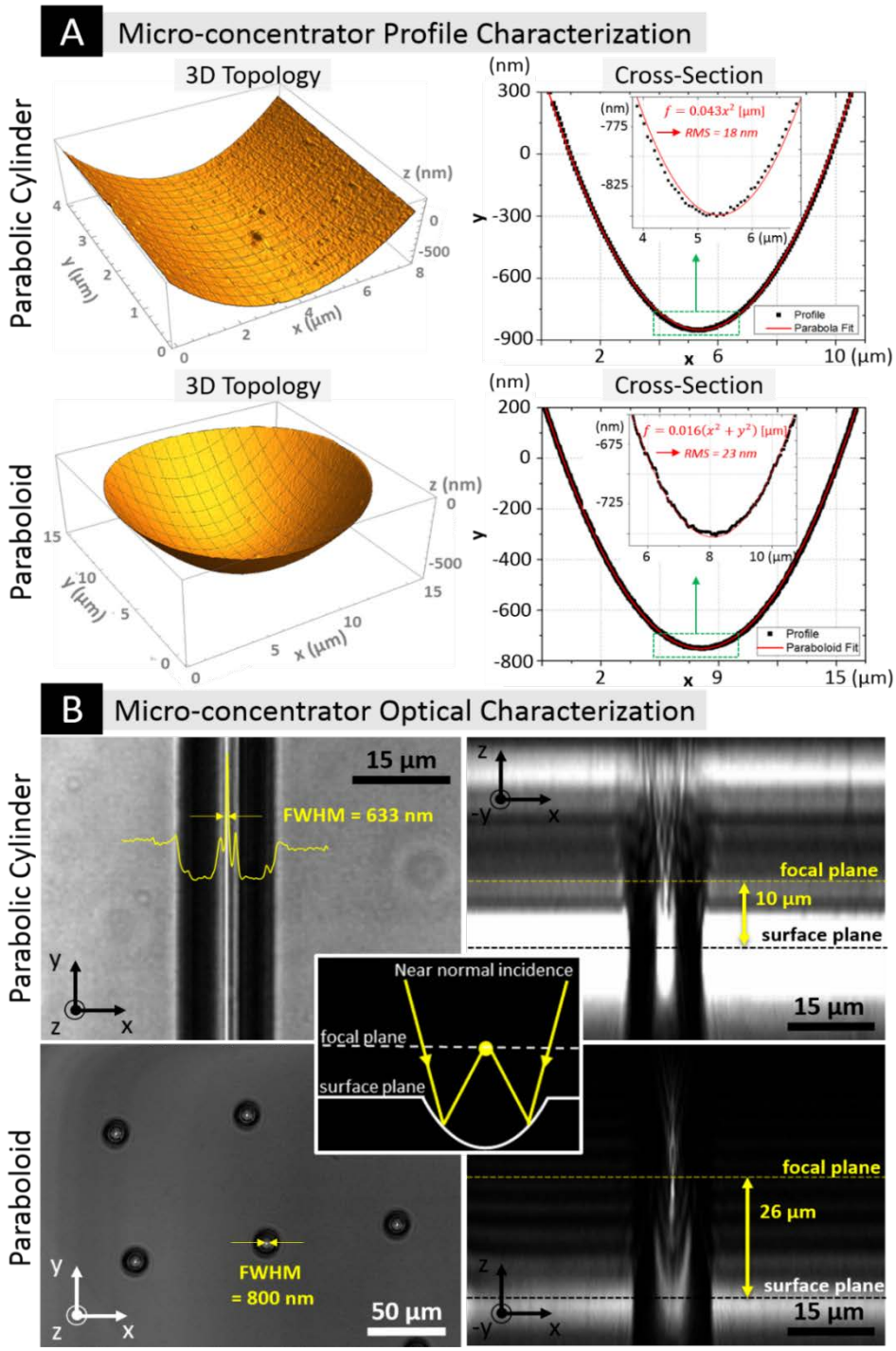

Figure 35: Profile and optical characterization of microconcentrators manufactured into p-Si. In part (a) and (b), the top and bottom rows depict data corresponding to parabolic cylinder and paraboloids, respectively. In part (a), AFM scans of the substrate (left) and its cross section (right) are ploted along with the fitted parabolic cylinder or paraboloid equation (only curvature term is displayed). In part (b), the left images depict an optical section of the reflected light (405 nm) image in XY plane together with the intensity distribution (yellow line inset) at the focal plane of the parabolic cylinder or paraboloid highlighting its tight focal spot and a cartoon (inset) showing the incident light angle interacting with the parabolic surface, and the right image showing the intensity distribution along the XZ plane of the reflected light image highlighting the XY plane where the focal spot is located and the shape of the intensity distribution confirms the parabolic shape of the cavity.

4.6 Future Work

Many of the issues with scaling the MACE-imprint process can be solved by improving the stamp and imprint tooling system. Further investigation into the chemistry and polymer science of stamp-solution interaction may prove beneficial. By studying robust stamp materials that (a) are chemically resistant to hydrofluoric acid and hydrogen peroxide, (b) can withstand mechanical cyclic loading of multiple imprinting cycles, and (c) are flat and compliant to avoid stress concentrations, the process should be able to achieve higher imprinting fidelity and repeatability. Similar issues are commonly found in, and have been addressed by, tooling systems for nanoimprint lithography (NIL) [88, 164, 89]. With Mac-Imprint, the chemical resistance is an additional design consideration. Unlike NIL, this process only requires contact for etching to occur and a light pressure is used to make conformal contact. Interestingly, these challenges open up areas for future work to improve this process and make it practical for an industrial scale imprinting process for porous silicon. Ultimately, the engineering of “in situ” process monitoring for precision control of feature depth, and precision alignment for both tilt and overlay registration will be required for this process.

4.7 Chapter Summary

Mac-Imprint demonstrates, for the first time the ability to imprint and pattern porous silicon without the need for mechanically crushing the porous material to be removed. As a result, it is capable of producing well-defined non-planar features with mirror quality surfaces. Because of differences in configuration that influence the transport of reactants and the cathodic and anodic reactions, the MACE-Imprint process behaves differently from the thin-film catalyst

MACE process. The process exploits the existing network of pores in the material to transport reactants to the stamp-substrate interface, localizing the etching of silicon at it, and accomplishing the imprinting of the stamp geometry into the substrate with sub-20 nm resolution. The porous material is capable of sustaining mass transport of reactants over length scales of several 10's of microns and, thus, localizing the etching. Material removal rates were observed to drop when a large enough volume of reactants was not locally available or the thickness of the porous layer approached the depth to which imprinting is performed. Thus, for implementing MACE-Imprint, careful considerations of how to locally store and periodically resupply reactants to the vicinity of the stamp-substrate interface are necessary. The large and changing difference in the effective areas of the cathode and anode require careful consideration of the composition of the etch solution. The absence of reactant diffusion can lead to non-localized pore formation that can change or destroy the morphology of the substrate. Notwithstanding, these technical challenges, MACE-Imprint brings new capabilities for imprinting and patterning of mesoporous silicon. It is capable of imprinting curved surfaces as was demonstrated by the fabrication of parabolic micro-concentrators with widths of 15 μm capable of focusing light to a spot whose FWHM was a factor of about 1.5 the input wavelength. Further, it has potential as a high through-put, economical process by avoiding lithography steps during production through the reuse of the imprinting stamp. Given the increased interest in porous silicon in biosensing [134] and in micro-optics as photonic crystals [23] and microcavities [15], and the inability of conventional lithography-based processes to pattern it, Mac-Imprint provides an important missing capability in potential manufacturing pathways.

Chapter 5. Silicon Electrochemical Imprinting with the Use of Porous Stamps

Anisotropic wet etching is considered the most economical top-down route to patterning single-crystal semiconductors that, traditionally, relies on differential etch rates of specific crystal planes. In contrast, catalyst-based wet etching (i.e. metal-assisted chemical etching) offers control of etching directionality that is contact-based and only weakly dependent on crystal orientation. By exploiting the later mechanism, this chapter demonstrates an electrochemical nanoimprinting process for single-crystal semiconductors for directly carving 3D features into single-crystal silicon wafers. While much of the work in chapter 0, focused on imprinting porous silicon substrates with solid catalysts, this chapter focuses on understanding the role porous catalysts play in enabling diffusion of chemical species during imprinting which, in turn, allows for morphology control of imprinted silicon features with sub-10 nm resolution in 3D. This process delivers low-defect density, and large-area patterning (>1 cm^2) in a single imprinting operation. Further, it outperforms the resolution and scalability of leading serial (e.g. FIB, electron beam) and parallel (e.g. gray-scale lithography) methods altogether by an order of magnitude, allowing for fast replication of patterns from a polymeric mold. This technique bypasses the need for dry etching and is potentially compatible with roll-to-roll platforms, amorphous and poly silicon, and III-V semiconductors. In turn, it may pave the way for the manufacturing of complex objects for infrared optics.

5.1 Overview

In a nanoimprint set-up (Figure 36a), a large-area catalytic stamp possessing 3D features and a pre-patterned silicon wafer are brought in contact while immersed in a MACE-specific etchant. After sufficient time in contact, the stamp's 3D shape and nanoscale features are carved into the silicon substrate. Unlike previous unsuccessful attempts to pattern silicon (i.e. non porous) with solid thin-film catalysts, this chapter specifically investigates the effect that porous thin-film catalysts (Figure 36b and d) have on improving the morphology of imprinted features, including at its surface (Figure 36c and e). First, it was necessary to synthesize porous noble metal thin-film catalysts with tunable pore volume fraction (PVF) which is introduced in section 5.2. Next, porous catalysts used during imprinting yielded dramatic improvements to etching selectivity and pattern fidelity. Such improvements were correlated to the (i) catalyst porosity and (ii) geometry which are discussed in sections 5.3 and 5.4, respectively. Experimental trends are discussed in the context of existing literature on MACE, and diffusion through pore-networks.

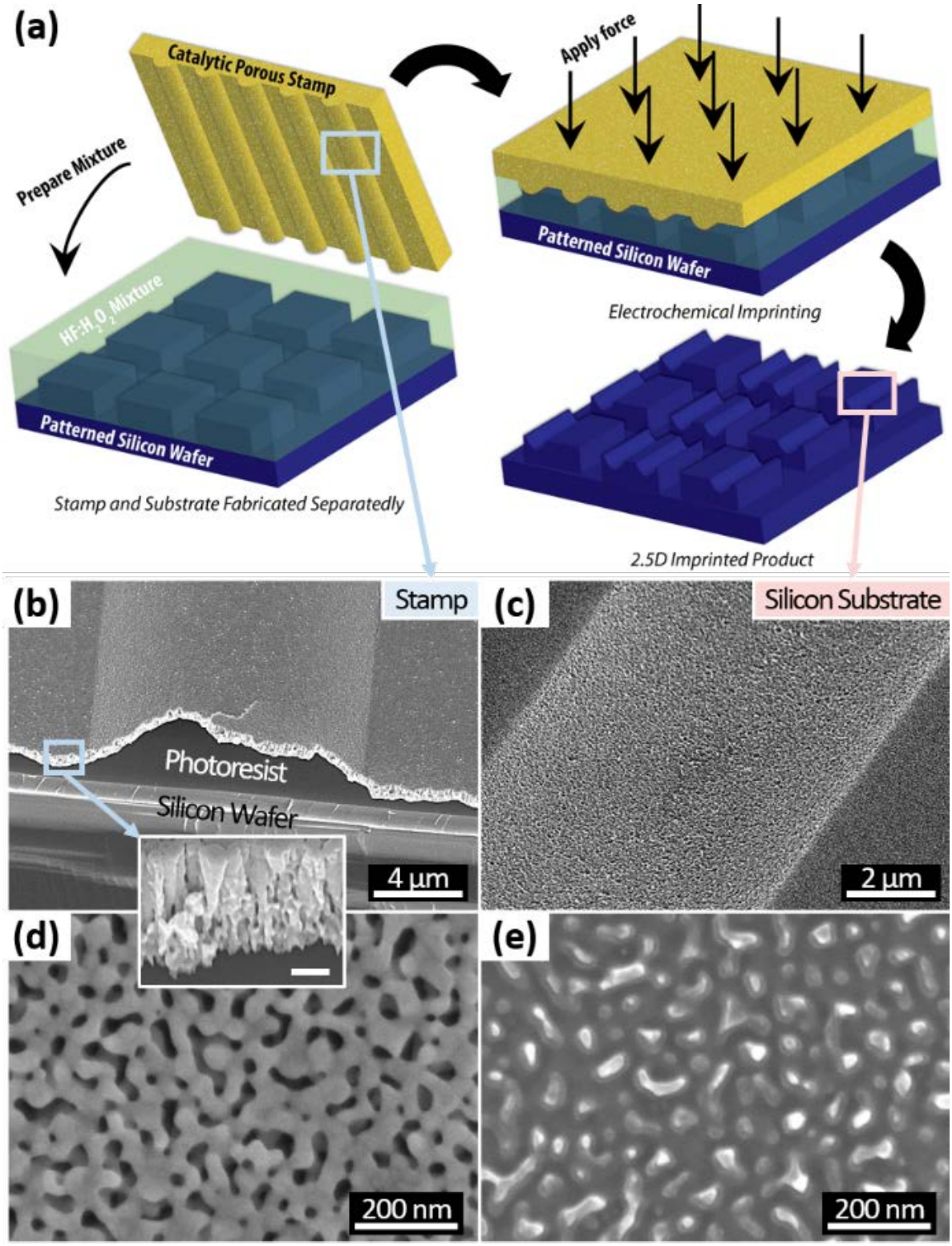

Figure 36: In part (a), the schematics shows a porous and permeable stamp being used to imprint features onto a pre-patterned silicon substrate. In part (b) and (d), the SEM depicts the tilted (by 30˚) cross-section and top-down of the stamp, respectively. The stamp is composed of a silicon substrate w/ a dewetted photoresist layer coated with a porous noble metal film prepared by co-sputtering and dealloying. In part (d) and (e), the SEM depicts the tilted (by 30˚) cross-section and top-down of the imprinted silicon surface, respectively.

5.2 Stamp Fabrication: Synthesis of Porous Gold Thin-Films

A well-established technique for preparing porous noble metal thin-films is dealloying in which the least noble element of an alloy is selectively removed by a wet etchant. Dealloyed thin-films possess varying average pore size and pore volume fraction depending on (i) dealloying conditions, such as anodization bias, temperature and time, (ii) chemical composition of electroless solutions, and (iii) relative content of the alloy elements [165]. This is possible primarily because of findings by Erlebacher et al. [166] who proposed that porous gold formation is initiated by the removal of a monolayer of the least noble element and formation of adatoms of the most noble element at the surface. Adatoms, being far more mobile than atoms in a crystal lattice, cluster into agglomerated islands by surface diffusion, reducing the total surface energy and reaching a less energetic meta-stable equilibrium state. Cycled over time, the etching front progress through the thickness of the film forming the pore walls and defining the pore structures [166].

5.2.1 Experimental Section

Stamps were fabricated similarly to the first procedure described in section 4.1.1 in Chapter 0. The method starts by spinning a 3 µm thick layer of AZ1518 photoresist (PR) supplied by MicroChemicals onto a 4 inch (100) Silicon wafer. This first layer was hard baked at 170 °C for 20 min and serves to protect the underlying silicon substrate. Next, a second layer was spun and patterned by lithography and also cured at 170 °C for 20 min, leading to dewetting of the second layer. The geometry of the patterns defined on the mask was fixed to an array of lines with 10 µm width and 128 µm spacing. After dewetting, the lines dewet into parabolic cylinders. Next,

stamps were co-sputtered with Ag and Au in an AJA Sputtering System calibrated with a crystal monitor. The deposition pressure was set to 3mTorr; the argon flow rate set to 4.5 sccm; the power in the Ag and Au targets were set to 95 W and 16 W, respectively, and its corresponding sputtering rates measured to be 3.5 Å/s and 1.2 Å/s. It is estimated from the relative sputtering rates that (a) volume fraction of silver is 0.75 (V_o) and (b) the film thickness is 400 nm. Finally, the films were dealloyed in a solution of nitric acid (70% diluted in water) and DI water mixed at 1:2 ratio, and kept at 60 ˚C ± 1 ˚C with a temperature controlled hot plate and constant stirring. To avoid uncertainty in the results due to variations of temperature and solution composition throughout the extent of the experiment, all samples are immersed simultaneously and removed after each specified etching time, thus, experiencing the same variations in the specified conditions throughout the experiment, minimizing relative errors. In Figure 37a, dealloyed films are shown displaying a gradient in color that varies from gray (after 10 seconds) to gold (after 30 seconds) and transitioning into varying degrees of red for longer etching times.

The pore volume fraction and pore size distribution of dealloyed films were estimated by (i) gravimetric analysis and (ii) analysis of SEM images, respectively. The former was performed using a microbalance (from Ohaus – model DV215CD) with 0.01 mg repeatability to weigh stamps before and after dealloying and its mass ratio (i.e. $MR = \frac{M_o - M_f}{M_o}$) plotted in Figure 37b. The latter was done on SEM images of porous films obtained with a Hitachi 4800 SEM. Image J software was used to analyze the pore size distribution whose average is shown in Figure 36b.

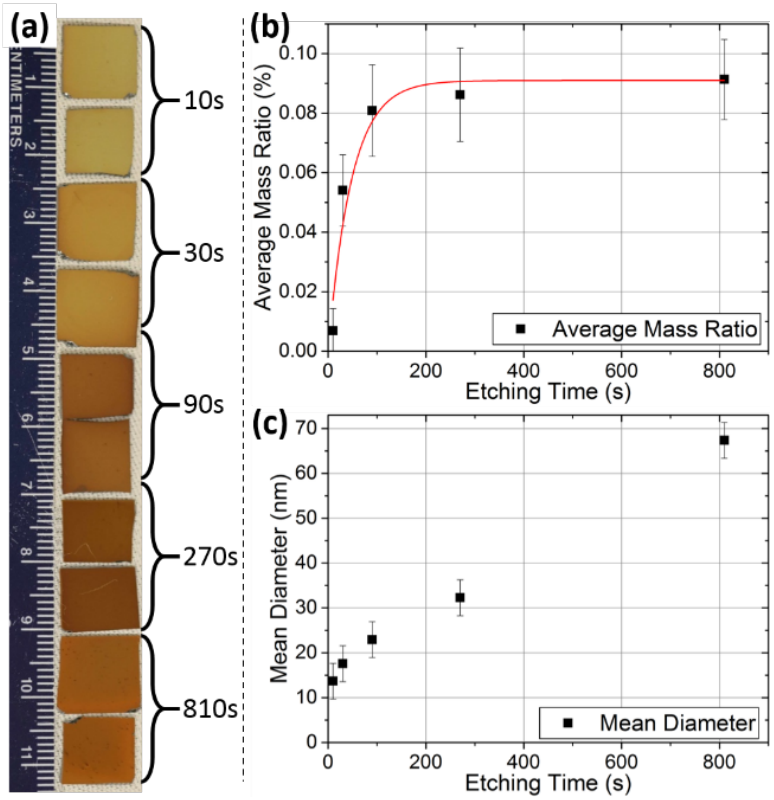

Figure 37: In part (a), porous stamps, cut into approximately 1x1 cm squares, are depicted in the photograph after dealloying for a specific etching time (denoted in the image). Part (b) and (c) are plots of the mass ratio and mean pore diameter of dealloyed Ag/Au films as a function of etching time obtained from gravimetric analysis and image analysis of SEM data, respectively.

5.2.2 Analysis of Gravimetric Data

In order to extract the pore volume fraction as a function of dealloying time, it was first necessary to analyze the mass data shown in Figure 37b. Since samples are cleaved into pieces that are not of identical dimensions, the data was analyzed in a scheme that eliminates the need for area measurements of each sample and the introduction of additional errors. Rather than using the difference of the initial and final mass which is dependent on sample size, it was chosen to compare the mass ratio because, as shown below, it is independent of the sample size.

Next, a formula for the mass ratio is derived. First, the initial mass (M_o) of the samples is defined as the sum of the products of the density (ρ_i), area (A_i) and thickness (t_i) of each layer (i.e. silicon wafer, photoresist, chromium and Au-Ag thin film) and it can be expressed as:

$$M_o = \left[\sum_{i=Si,PR,\,Cr,\,Au} \rho_i(At_i)\right] + \rho_{AgAu}\left(At_{AgAu}\right)$$

The density of the thin-film alloy can also be expressed as a function of the initial volume fraction of silver (V_o) as follows:

$$\rho_{AgAu} = \rho_{Ag}(V_o) + \rho_{Au}(1 - V_o)$$

Assuming that only silver atoms are etched during the dealloying step, the final mass of the samples (M_f) can thus be written as a function of the final volume fraction of silver in the alloy film (V_f):

$$M_f = \left[\sum_{i=Si,PR,\,Cr,\,Au} \rho_i(At_i)\right] + \left[\rho_{Ag}\left(V_f\right) + \rho_{Au}(1 - V_o)\right]At_{AgAu}$$

As a result, the mass ratio can be simplified to the equation below:

$$Mass\ Ratio = \frac{M_o - M_f}{M_o} = C_o\left(V_o - V_f(t)\right)$$

$$where\ C_o = \frac{\rho_{Ag}t_{AgAu}}{\sum_{i=Si,PR,\,Cr,\,Au}\rho_i(t_i) + \rho_{AgAu}\left(t_{AgAu}\right)}$$

Note that this equation becomes independent of the area of the sample and C_o becomes a fixed parameter dependent only on the initial characteristics of the film. Also, the difference

V_o-V_f is the apparent pore volume fraction (i.e. volume of pores divided by the initial volume of the film), which neglects morphological changes of the thin-film during dealloying (such as shrinking). Next, the following empirical formula, in which C_o and k are fitting parameters, was used to fit the mass ratio data in Figure 37b. This formula was selected not only because it fits well the data, but also because it converges to a fixed and maximum value (i.e. V_o) which agrees well with the notion that silver is completely removed at sufficiently long etch times:

$$\frac{M_o - M_f}{M_o} = C_o V_o (1 - e^{-kt})$$

The apparent pore volume fraction can be extracted from the curve fitting and is recorded in Table 2.

Table 2: Apparent Pore Volume Fraction Determination

Correlation of Dealloying Time and Pore Volume Fraction of Porous Gold Films					
Time (s)	10	30	90	270	810
Apparent Pore Volume Fraction (%)	17.4	41.0	68.0	74.9	75.0

5.2.3 Discussion of Dealloying Results

By selecting a lower temperature and diluting the etchant during the dealloying step, the rate of silver removal is reduced by an order of magnitude in comparison with results from recent literature [167]. As a result, it became possible to partially dealloy porous films with tunable apparent pore volume fraction by timing the etching step. It is observed that the apparent pore volume fraction increases in time at a rate that exponentially decays with increasing dealloying

time (Figure 37b). This trend indicates that the silver content of the film is completely removed after 810 seconds.

Additionally, the average pore size is also not constant and it increases with etching time. Initially, it increases at a fast rate during a period of 10-20 seconds, and, thereafter, it increases linearly at a slower rate. The initial formation of small pores (< 5 nm) is driven by the Au adatom formation and diffusion into clusters that over time extend through the thickness of the alloy. However, as time progresses, pores are continuously enlarged and coalesce with neighboring ones forming large pores (up to 70 nm) (see Figure 37c) which is a phenomena that deserves more detailed studies. It seems probable that the pores coalesce due to curvature-driven surface diffusion similarly to the mechanism that drives thin-film dewetting.

5.3 Substrate Morphology Dependence on Stamp Porosity

In order to establish a direct comparison, silicon substrates (p-type and with resistivity in the range of 1-10 ohm.cm) were imprinted with porous and solid stamps under identical experimental conditions as the experiments described in section 4.1.3 (i.e. ρ = 96%, force = 4 lbf, and time = 3 min). In previous unsuccessful attempts (shown in Figure 26a), solid catalysts produce features in silicon without any discernible pattern fidelity (i.e. shapes of stamp and substrate do not match) and etching is delocalized from the catalyst-silicon interface. In contrast, pattern fidelity is restored with the use of highly porous stamps (Figure 36e and Figure 38) and etching is localized, leading to patterning resolution in 3D as small as 10 nm (Figure 36e).

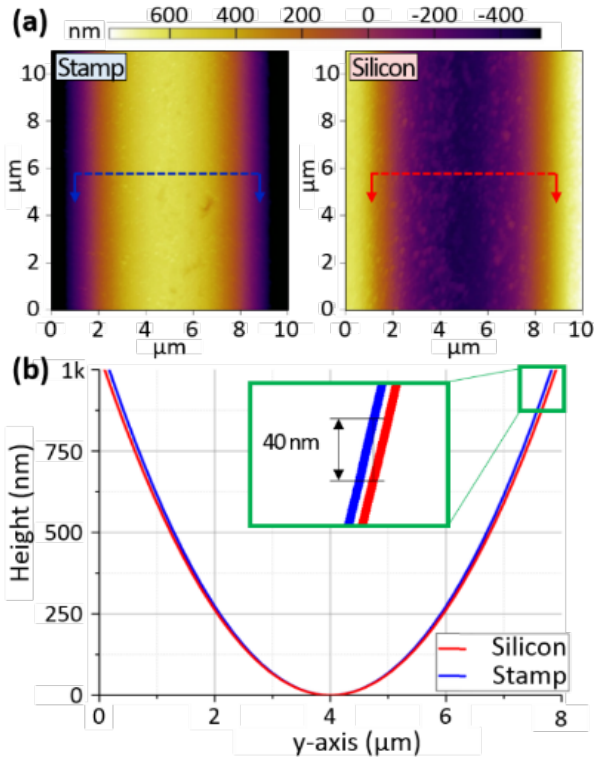

Figure 38: In part (a), the topology of stamp (left) and substrate (right) is measured via AFM at complimentary locations. Porous stamp with high pore volume fraction (>68%) was used during imprinting in this case. In part (b), the cross-section profiles of stamp and substrate (marked by color in part (a)) are superimposed to highlight accurate transfer of shape during imprinting.

This dramatic increase in pattern fidelity with the use of porous stamps can be explained by existing literature on (i) MACE and (ii) diffusion through porous networks. When Chartier et al. [81] performed the etch rate measurement as a function of the ρ-parameter, the experiment was performed with nanoparticles whose size was in the 10-30 nm range. At this length scale, diffusion pathway to the center of the catalyst-silicon interface is short and diffusion towards the catalyst-silicon interface is presumably not the rate-limiting step. Thus, the argument that, at ρ=75%, the etch rate is maximized due to the stoichiometry balancing of the proposed reaction mechanism holds true. However, Geyer et al. found that - for larger features sizes (i.e. > 500 nm) and thicker thin-film catalyst (i.e. > 30 nm) - the etch rates were significantly lowered and a porous silicon layer was formed underneath and around the catalyst to support mass transport

of ionic and inert species to and from the center of the features [78]. These results support the idea that diffusion of reacting species becomes the limiting-rate step when the diffusion pathway is sufficiently large or the catalyst film does not allow for fast diffusion through its thickness.

The difference in the imprinting morphology obtained with solid and highly porous catalyst (i.e. PVF > 68%) is analogous to the observations of Chartier et al. and Geyer et al. Utilizing nanoporous catalysts in MACE is a way to increase the effective diffusion coefficient of the catalyst thin-film and reduce the diffusion pathway. That is because, when a contiguous pore network is formed in a porous polycrystalline metal thin-film, molecules and ions diffuse not only through its grain boundaries and bulk grains, but also through the void phase. Although highly tortuous, this void phase possesses a diffusion constant that is orders of magnitude higher than that of grain boundaries [168]. This is due to the fact that grain boundaries are highly tortuous and narrow (i.e. width is in the length scale of the electrical double layer thickness) which constraints ion mobility and, thus, possess a lower effective diffusion constant. In mesopores, the molecules weakly interact with the pore walls since the pore sizes are much greater than the electrical double layer. As a result, imprinting with highly porous catalyst promotes diffusion and leads to well defined features during imprinting and no formation of pores in the silicon substrate.

To further validate this point, imprinting was performed with partially porosified stamps with a wide range of PVF from 17% to 75% (Figure 39 and Figure). In the case of PVF=17%, the electrochemical reaction is highly unlocalized, leading to the formation mesoporous silicon and loss of pattern fidelity. A sharp decay in the rate of porous silicon formation takes place when

PVF reaches 68% and sub-30 nm features from the stamp appear on the substrate (shown in Figure 39). This observed transition (i.e. from delocalized to localized etching) can be best explained by the restoration of the diffusion of reacting species from the edge to the center of the contact interface. According to the random network theory, a continuous network is formed when PVF is approximately 50% [168]. Thus, imprinting with highly porous stamps at high ρ-values (i.e. >75%) leads to localized etching and minimizes porous formation which matches the results previously obtained with solid catalysts with short widths (< 50 nm). Additional evidence of this effect is presented in "Appendix E: Silicon imprinting with porous catalysts".

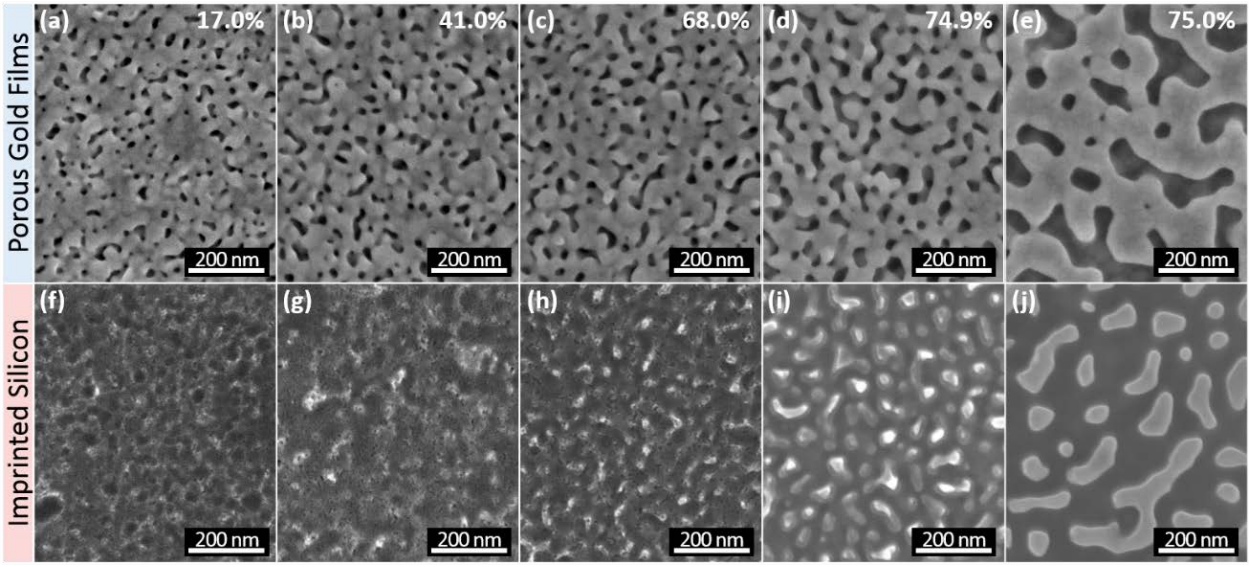

Figure 39: Comparison of stamp and substrate morphology via top-down SEM images. The top row shows the detailed morphology of partially porous catalyst films and, on the top-right corner of each image, the apparent pore volume fraction (derived from the gravimetric analysis of dealloyed films) is noted. The bottom row depicts the morphology of the imprinted silicon substrate which was imprinted with the porous catalysts corresponding to its column item directly above it. As the stamps become more porous, the features are more clearly defined on the substrate with high-detail of sub-10 nm features.

5.4 Substrate Morphology Dependence on Catalyst Geometry

Unlike thin-film based MACE, in imprinting formats, the ratio of the area of the cathode (i.e. gold surface exposed to MACE solution) and the contact area between the catalyst and

silicon (A^*) is not restricted to unity and it can vary depending on the catalyst geometry. For instance, by simply increasing the overhanging portion of the catalyst, the cathode area is extended along catalyst solution interface while the contact area remains unchanged (as in Figure 40a). If the cathodic reaction scales with the cathode area, then, in theory, the rate of hole injection into silicon can be increased as well, modifying the etching morphology of imprinted features. Thus, this section examines the hypothesis that the reaction kinetics is modulated by the geometry of the catalyst.

To test this hypothesis, Mac-imprint was performed with roller stamps possessing overhanging domains sufficiently large to vary A^* (equal to w_s/w_c in the configuration shown in Figure 40a) by an order of magnitude. This was accomplished by sputter coating plastic sinusoidal gratings with gold films through a shadow mask possessing varying widths (i.e. 2, 6, 12 mm). The plastic grating was wrapped around a Teflon rod, loaded onto a Z-stage and fully submerged in a solution of HF and H_2O_2 (ρ = 75%). Imprinting was performed at the set point load for 10 min for all trials and imprinted silicon substrates were rinsed in DI water for 3 min afterwards.

Subsequently, gravimetric analysis was employed to determine the total mass of silicon removed during imprinting as a function of the shadow mask width (w_s). It is observed that the total mass of silicon removed scales linearly with the shadow mask width while the contact width (w_c) remains constant (Figure 40b). Thus, by keeping the solution parameter, temperature, time, and pressure constant, and only varying the catalyst overhanging length of the catalyst, it is demonstrated that the apparent removal rate of silicon increased which constitutes the first

evidence in MACE literature that the catalyst geometry plays a role in regulating the kinetics of hole injection.

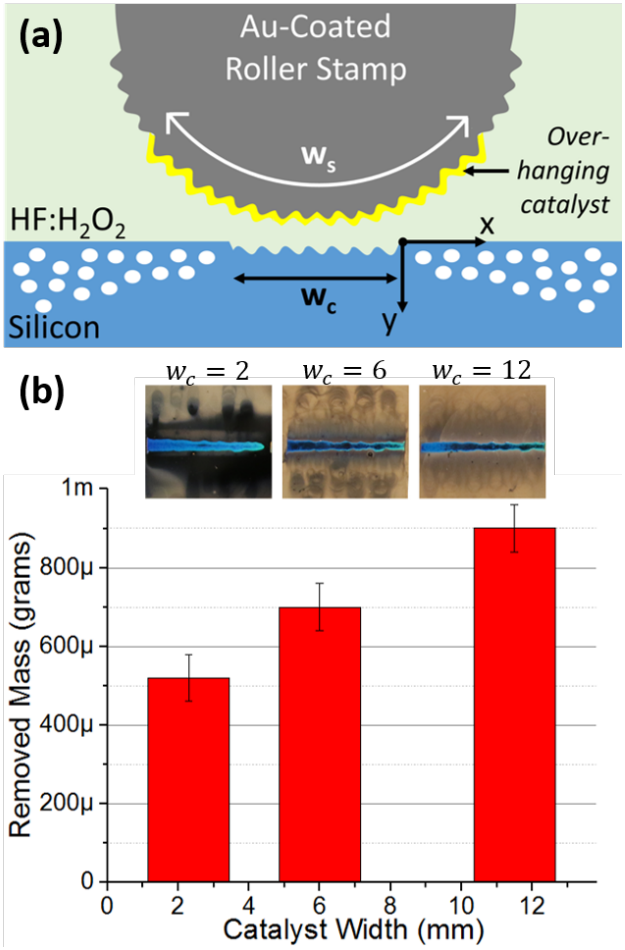

Figure 40: Silicon removal as a function of catalyst width. Part (a) shows a schematic of the imprinting set-up with a roller stamp. The roller stamps possess a overhanging structure that allows one to vary the catalyst-solution interface area independently of the catalyst-silicon interface area. Part (b) shows the removed mass obtained from gravimetric analysis of imprinted silicon substrates as a function of catalyst width (w_c). Inset images are optical top-down images of the imprinted domain showing the blue reflection of the imprinted grating line (note that the surroundings are heavily porosified due to the use of solid catalysts.

5.5 Chapter Summary

In summary, Mac-imprint has been extended to silicon wafers (i.e. non porous) with the use of porous catalysts. It has been shown that catalyst geometry and porosity are relevant factors in nanoimprinting with MACE-based solutions to reduce the diffusion pathway, increase

the effective diffusion constant of the porous metal catalyst, and regulate reaction kinetics. Further, it has been shown that the relative area ratio of catalyst-solution to the catalyst-silicon interface plays an important role in regulating the morphology of imprinted silicon substrates as well. Combined, these factors capture the unique considerations one must have when using the Mac-imprint technique for generating pristine features into silicon and, potentially, other semiconductors.

Chapter 6. Conclusion

This thesis introduces new capabilities to semiconductor nanomanufacturing. First, it introduces new processes for manufacturing high-quality 1D and 3D silicon nanostructures via (a) self-assembly and wet-etching, and (b) electrochemical nanoimprinting, respectively. Second, it provides rich datasets and analyses to understand the fundamental mechanisms governing and limiting material removal and assembly.

On electrochemical nanoimprinting, the primary finding of this work is that metal-assisted chemical etching can be regulated by the diffusion of reacting species. It was shown that nanoporous materials can sustain mass transport of reactants and products either through the substrate or stamp. In either case, the morphology of imprinted nanostructures is regulated by the characteristics of the porous materials such as its thickness and pore volume fraction. When the porosity is sufficient to form a percolated network of pores, it sustains a fast mass transport and, consequently, electrochemical nanoimprinting produces pristine silicon nanostructures without the concomitant porous silicon formation which is highly undesirable and detrimental to the optical and electrical properties of the substrate. Additionally, this work highlighted the importance of the catalyst geometry in regulating reaction kinetics in electrochemical imprinting. As a result, patterning of porous silicon and silicon substrates is attained with minimal damage to the substrate's original crystal morphology and with sub-20 nm resolution. Although powerful, electrochemical nanoimprint cannot sustain constant etch rates indefinitely and existing nanoimprint equipment does not support in-situ monitoring and control of this process.

On self-assembly, the primary finding of this work is that thin-film dewetting can spontaneously produce dot-patterns whose size and areal density are regulated by external parameters. Further, thin-film dewetting was employed for decorating 1D nanostructures (such as SiNWs) with metallic nanoparticles and produce complex hybrid silicon-metal nanomaterials. This work on thin-film dewetting is marked by the mapping of the film deposition and annealing conditions to the particle size, contact angle and areal density of nanoparticles. Finally, it is determined that even below the eutectic temperature on the silicon-metal nanomaterial systems, the contact angle is regulated by temperature and particle size, which is a new finding in the scientific literature. It is suggested that atomic mixing across the metal-silicon interface and the size-dependent cohesive energy of nanoparticles regulates the contact angle dependence on temperature and particle size, respectively.

In summary, combining innovative manufacturing stratefies and a fundamental knowledge of nanoscale processes leads to breakthrough improvements in scalability, cost and dimensional control in nanomanufacturing of semiconducting materials which are relevant for applications in energy, defense, healthcare and communications. Process monitoring and control for electrochemical reactions and self-assembly is still incipient and motivates a direction forward towards concomitant automation and modeling of such processes. If an automated and reliable platform for nanomanufacturing of silicon materials can be designed, a wider span of applications of nanomaterials will become feasible. For instance, electrochemical nanoimprinting may be extended to a wider range of semiconductors and potentially be used for manufacturing of complex optical materials; and self-assembled hybrid silicon-metal nanomaterials may be used in artificial photosynthesis and biomedical applications.

Chapter 7. References

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Appendix A: Silicon nanowire diameter distribution analysis

A1 Using Image J for analyzing particle size

As shown on Figure A1, all samples were analyzed under SEM with the samples mounted horizontally. Scanning Electron Microscopy data was adjusted for threshold using Image J and particle area for each particle was measured. Assuming perfectly rounded particles, the diameter was derived and results have been summarized and reported in this document. Each row in the figure below represents a stage of the image analysis. Samples were obtained by loading each for an individual evaporation round with the thickness and evaporation rate being monitored directly by the crystal quartz monitor for all samples.

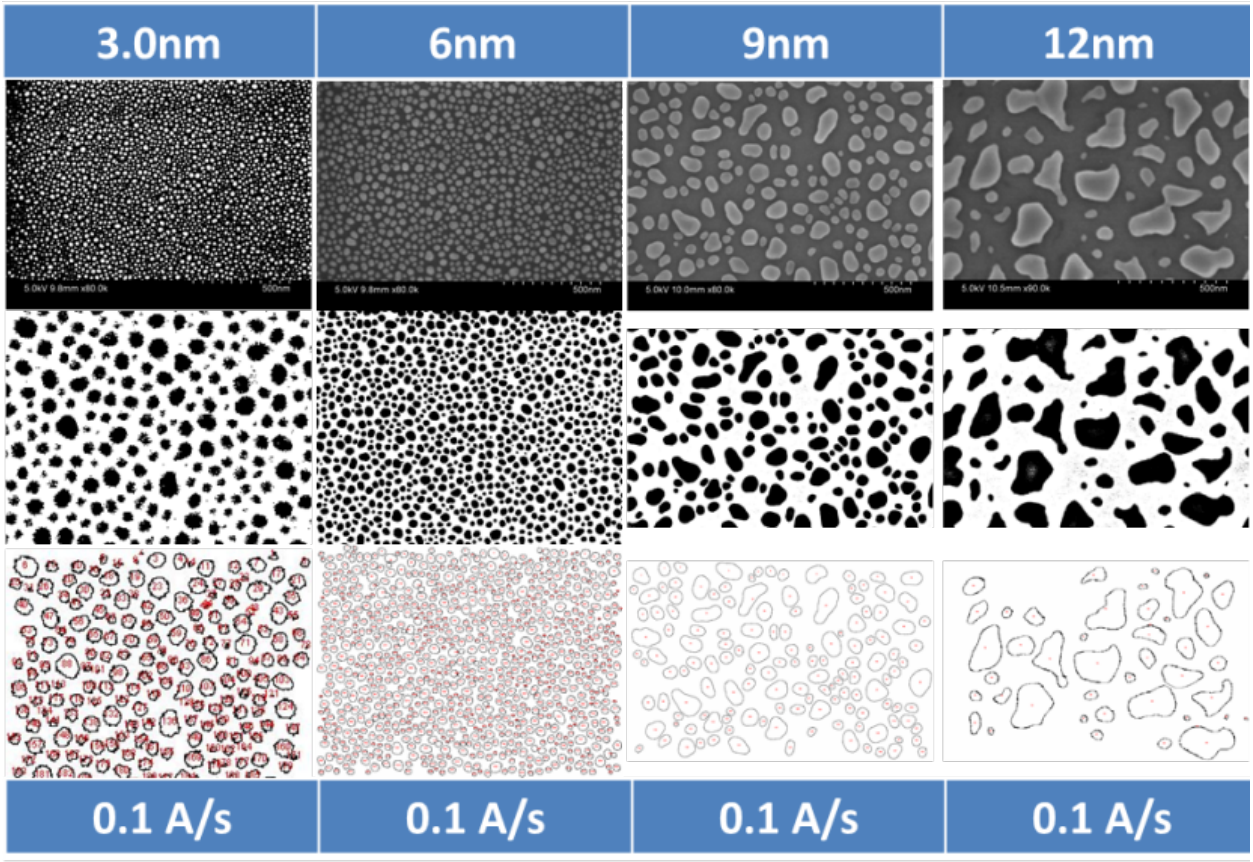


Figure 41: Image analysis step-by-step. The first and last row display the evaporation parameters for thickness and deposition rate of the silver film, respectively. And, the second, third and fourth rows display the corresponding raw scanning electron micrograph image of dewetted silver particles, the black and white image generated after applying a contracts threshold, and the highlighted particle contour of the data analyzed via image J.

Appendix B: Silicon nanowire tapering: characterization and image analysis

The taper characterization used high-magnification SEM images of SiNW cross-section as shown in Figure B1 below (left, [EtOH]=13.7 and right, [EtOH]=14.61). Images were loaded into free-software GIMP for manual measurement of the taper at the base of the wires.

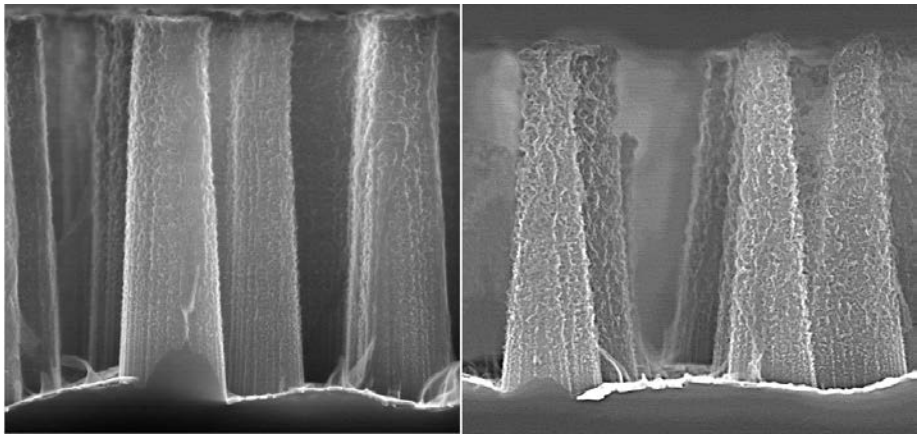


Figure 42: Taper angle dependence on ethanol concentration

Appendix C: Silicon nanowire roughness characterization

C1 Reducing The Etch Rate of Metal-Assisted Chemical Etching

In the selection of MacEtch solution for roughening of SiNWs, we sought a solution with reduced etch rate and no excess holes being produced as to avoid porous formation. Silicon chips patterned with a gold mesh were immersed in MacEtch at a ρ=75 and for varying degrees of water content. Note that this parameter is defined in literature [81] as the molar concentration of HF divided by the sum of the molar concentration of HF and H_2O_2. No pores were observed in the SiNWs for the entire water molarity range studied. The etch rate was reduced by almost 3 orders of magnitude as shown in Figure C1.

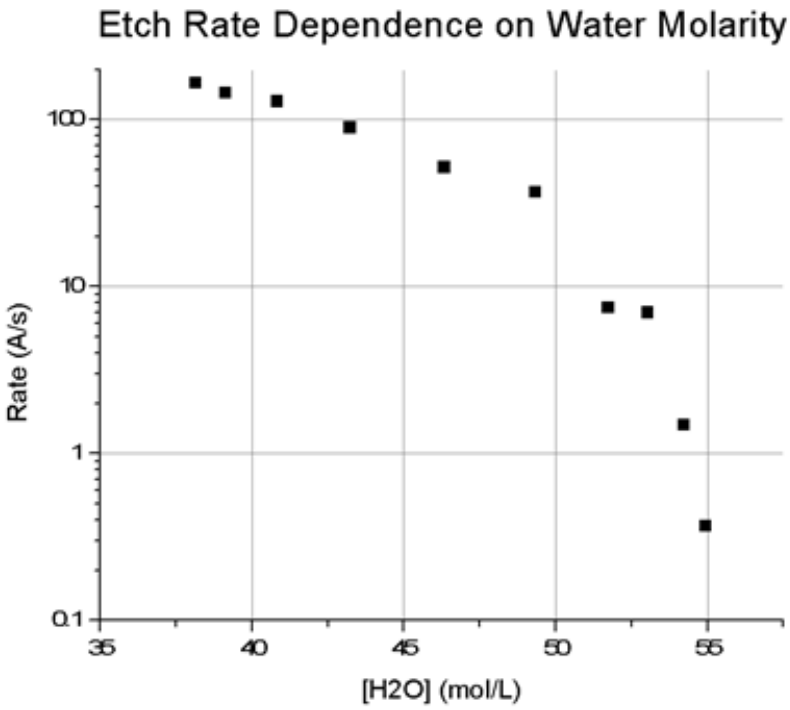


Figure 43: Etch rate dependence on water molarity

C2 Roughness Analysis from Transmission Electron Microscopy Data

For roughness characterization of the nanowires, we disperse the nanowires on holey carbon grid. A double-tilt holder is used to align the nanowire with [110] zone axis to obtain atomic resolution images. The diffraction pattern of the roughened nanowires reveals the single-crystallinity on Figure C2.

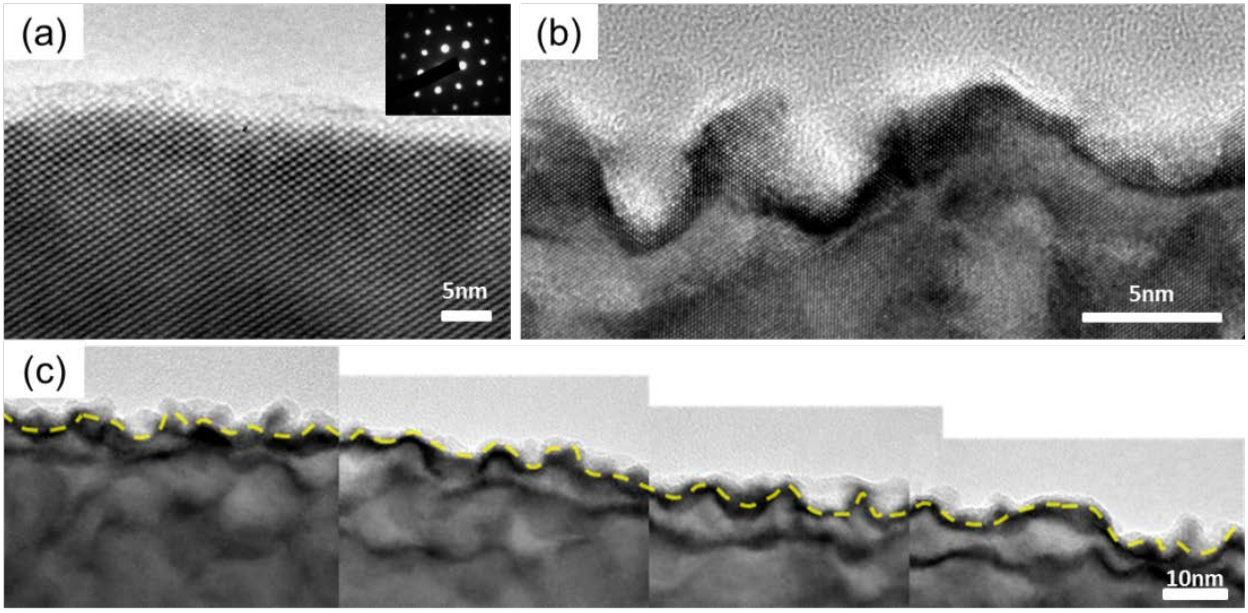


Figure 44: Details on TEM analysis - The surface contour tracking of Si/SiO_2 boundary from HRTEM images using Image J.

In order to construct the roughness profile of the sidewall, we take several continuous images along the boundary of the wire. The Si/SiO_2 atomic boundary is traced out in every image using ImageJ and the resulting profiles are stitched into a continuous surface. The mean surface of the boundary is obtained by a linear fit to the stitched profile. The roughness height ($\zeta(x)$ where x-axis is along the length of the wire) is defined about this mean surface and the standard deviation of $\zeta(x)$ yields the root-mean square (RMS) roughness height. We conduct this procedure

with at least three nanowires from the same sample to obtain a statistical mean RMS height as shown on Figure C3.

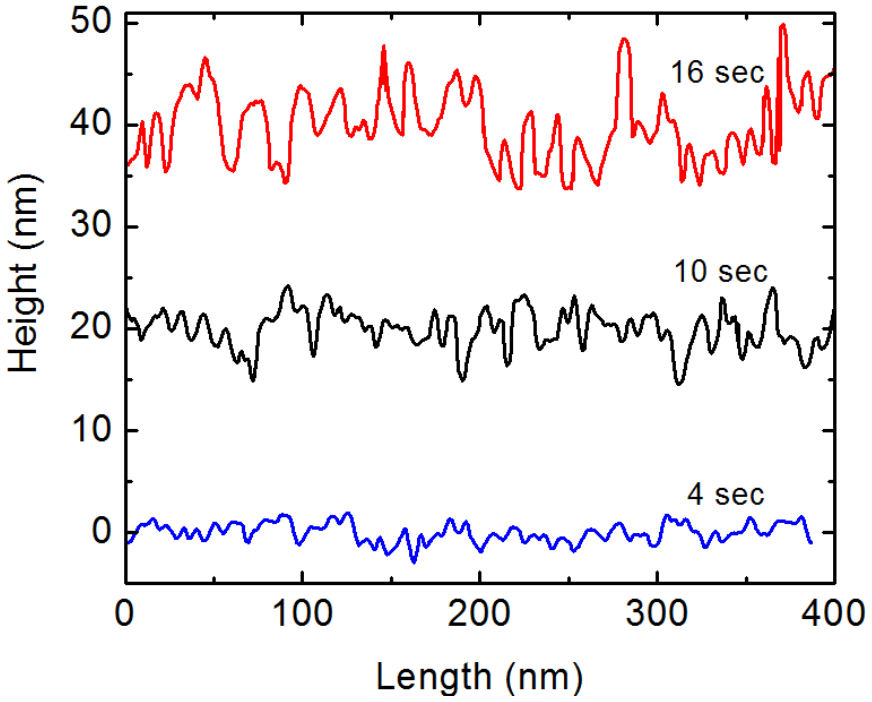


Figure 45: Details on TEM analysis. The surface roughness profile analysis of Si/SiO_2 boundary for different etch times imaged using HRTEM

Appendix D: Silicon Nanowire Production and Sample Records

The following samples were reproduced on 2-4 cm^2 Si chips. Table 3 summarizes the results obtained, showing the particle distribution, areal coverage, the lift-off yield and the as-fabricated SiNW sample. The results reported here have been repeated and are consistent.

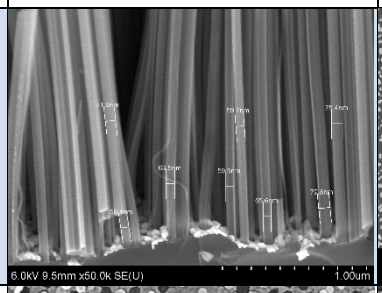
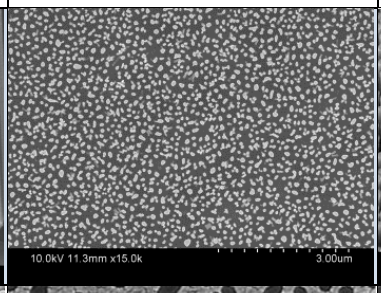
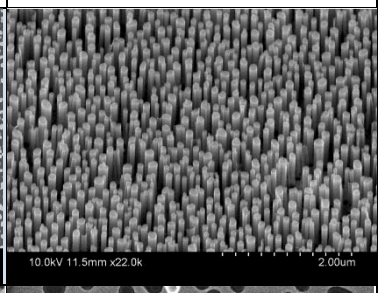
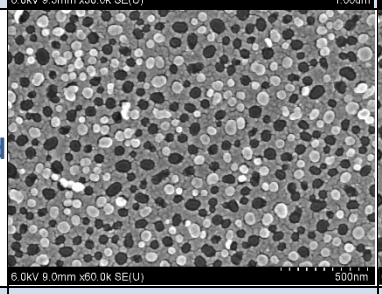
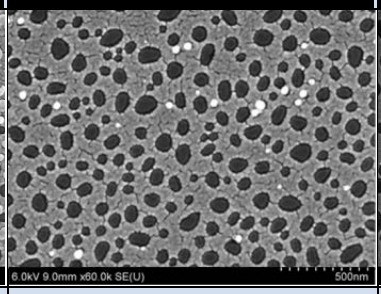
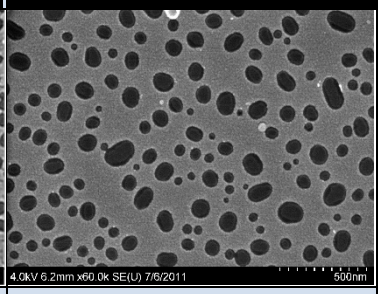
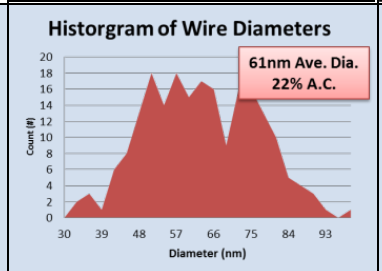
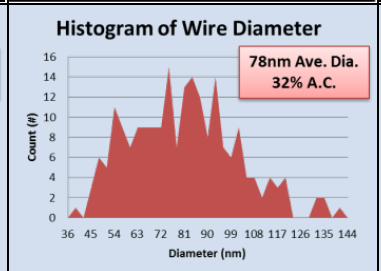
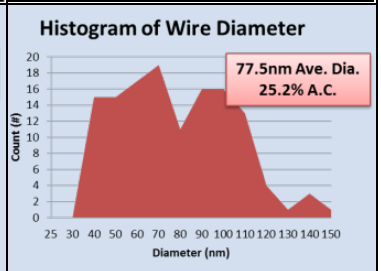
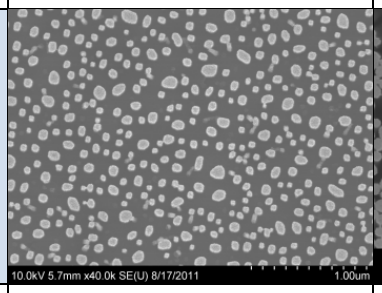
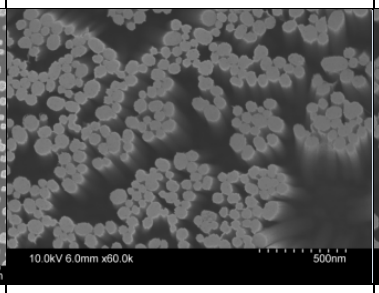
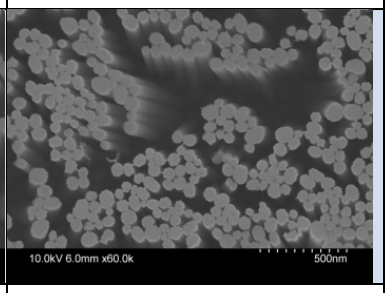
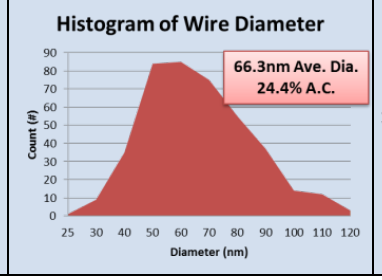
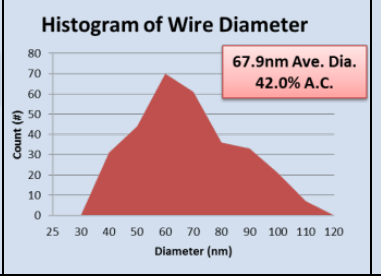
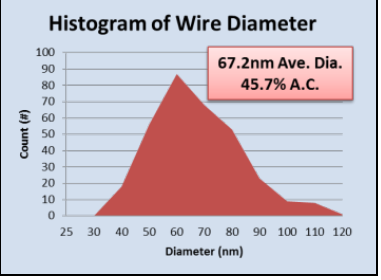
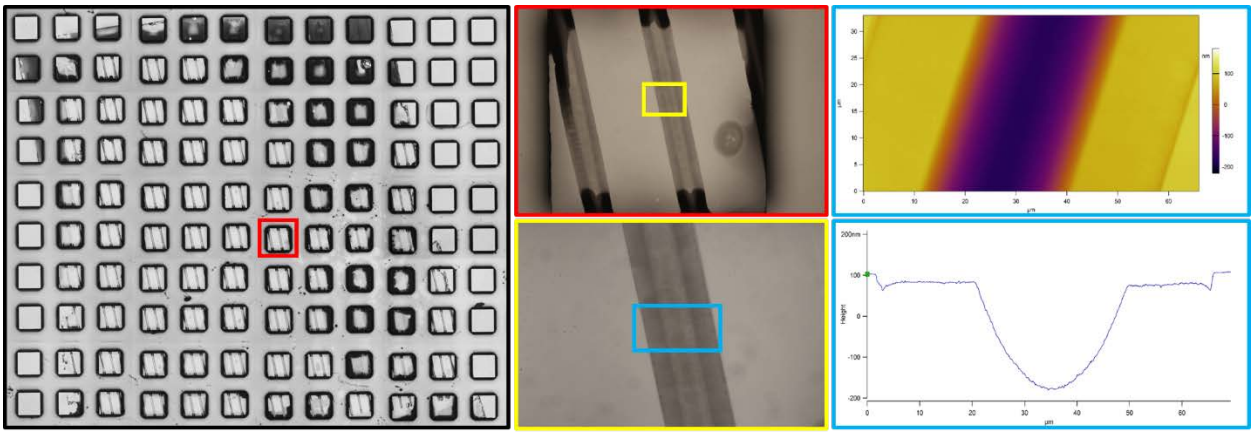
Sample Code	A-05/26/11	B-06/01/11	C-07/06/11
SEM of Wires			
Lift-off Yield			
Histograms			
Sample Code	D-08/17/11	E-09/28/11	F-09/28/11
SEM of Wires			
Lift-off Yield	>95%	>95%	>95%
Histograms			

Table 3: Sample records show the minimum particle size and maximum areal coverage obtained consistently.

Appendix E: Silicon imprinting with porous catalysts

In this supplementary section, more information about the experimental results of silicon imprinting with porous stamps is presented. First, the entire imprinted domains (i.e. approximately 1 cm^2) were imaged with an optical microscope at 2.5x and at select locations near the center of the imprinted domain at 20x and 50x (see Figure). Lastly, the imprinted feature topology was measured with AFM at selected locations. By overlaying optical and AFM results, it is possible to distinguish the imprinted domains (i.e. where the catalyst was in contact with the silicon substrate) from the porous silicon formation surrounding the features (see Figure 46).



2.5x optical image of entire imprinted area | *Imprinted area at select locations at 20x & 50x* | *AFM image of topology at select location*

Figure 46: Description of method of data collection of imprinted silicon substrates.

In section 5.3, it was stated that imprinting with low-PVF (i.e. 17-41%) leads to delocalized etching and porous silicon formation and, as the stamp becomes more porous (i.e. 68-75%), the etching is localized to the stamp-silicon contact interface. Additional evidence of this phenomena is presented in Figure 47; the 2.5x optical images of the imprinted silicon substrates are shown

and darkening of the substrate – which is indicative of porous silicon formation - was observed for low-PVF values (Figure 48) and long etching times (Figure 49).

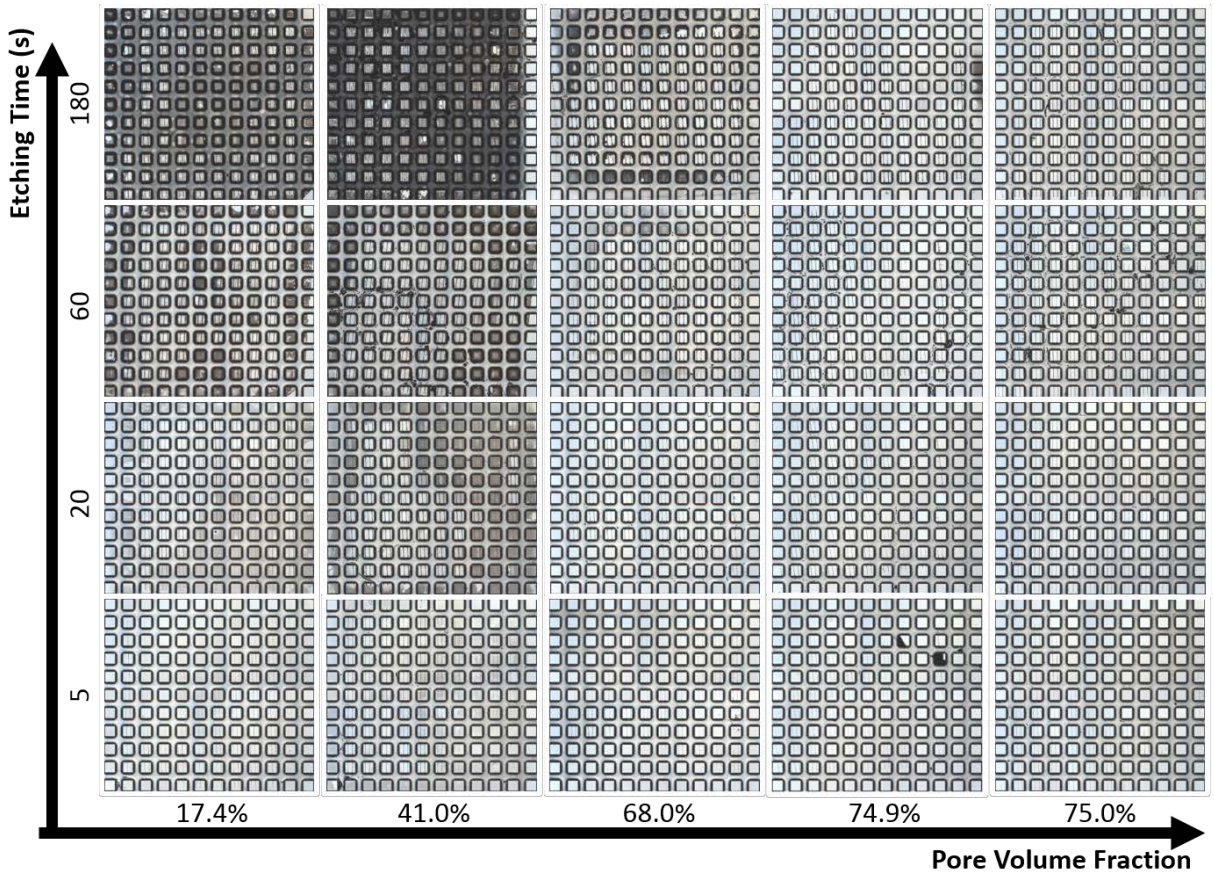


Figure 47: Optical images of entire 1 cm x 1cm domains with a 2.5x magnification with top-down illumination. Images are arranged as a function of the imprinting time and the PVF of the stamp used to imprint. All images are taken at the same light exposure conditions without contrast or brightness adjustments.

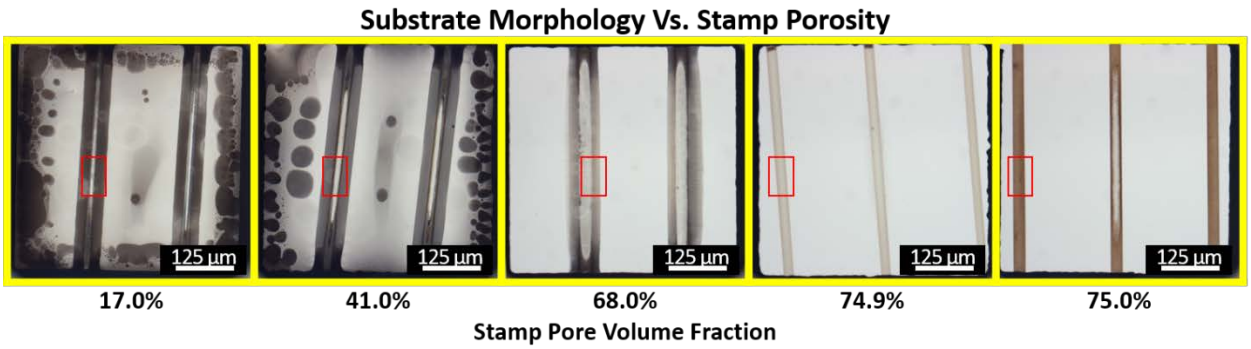


Figure 48: Optical image at 20x magnification of imprinted silicon substrates etched under ρ=98% and for 60s. Near vertical lines correspond to contact areas between stamp and substrate. Porous silicon domains form in the surroundings of the imprinted features. At lower PVF, porosification of the substrate is evidenced by the darkening of the silicon surface. All images are taken at the same light exposure conditions without contrast or brightness adjustments.

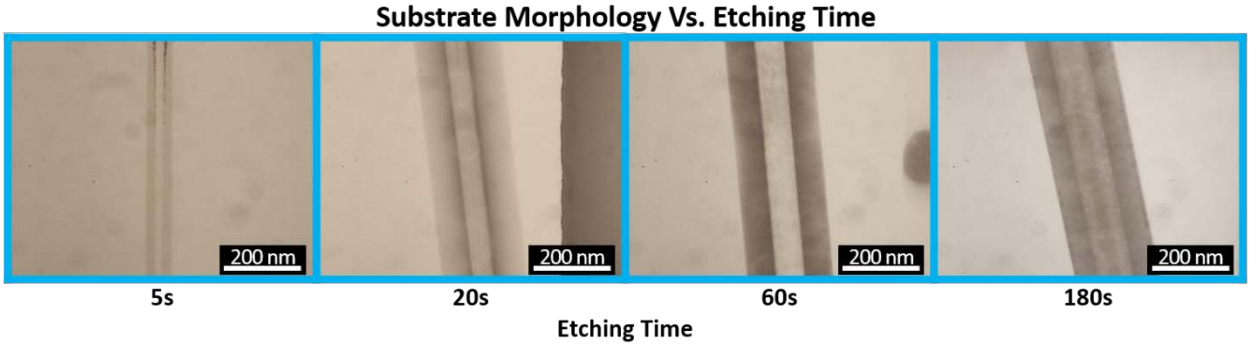


Figure 49: Optical images at 50x magnification of imprinted silicon substrates for different etch times at ρ=98% and PVF=68%. All images are taken at the same light exposure conditions without contrast or brightness adjustments.

Lastly, top-down SEM images of the features at selected locations were collected. In the case of PVF =41%, the images reveal the mesoporous nature of the silicon surface near the imprinted domain and in its surroundings (Figure). In the case PVF=75%, the SEM images do not reveal any mesoporous silicon and patterns are well defined resembling the features of the stamp (Figure).

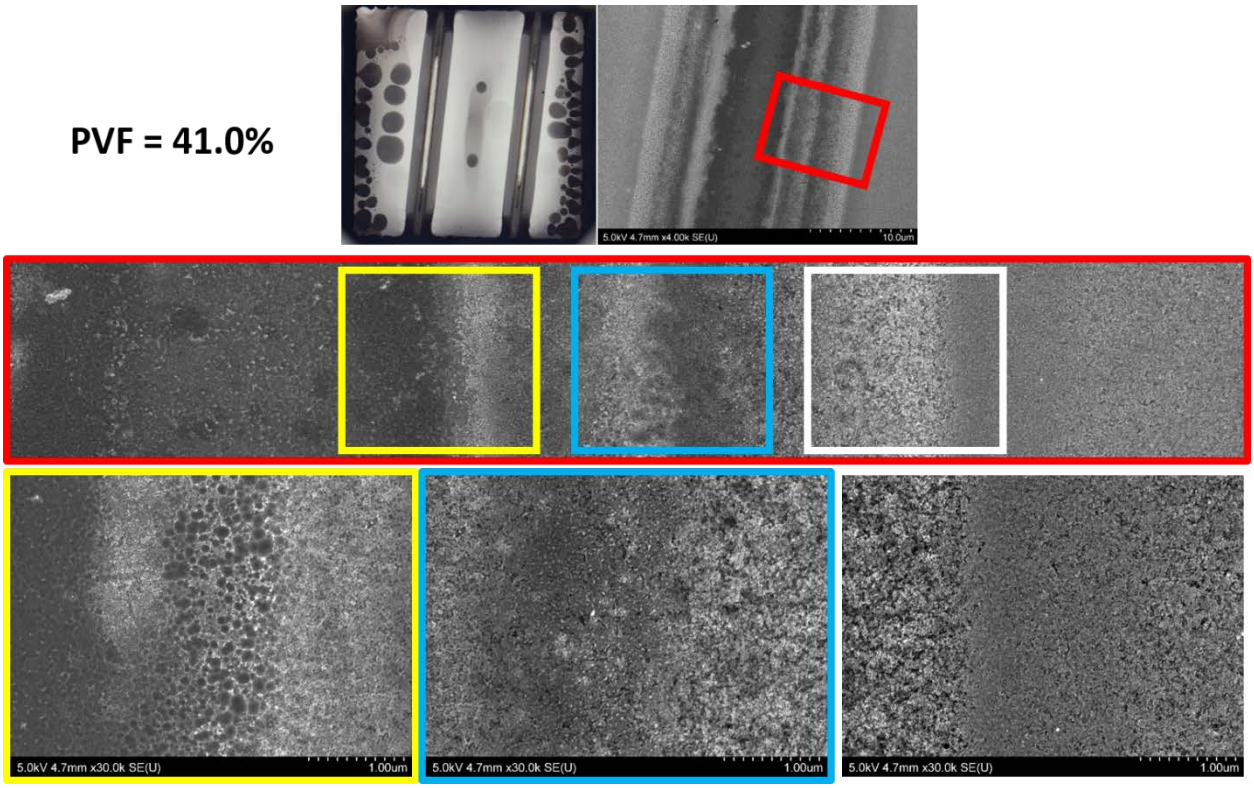


Figure 50: At the top row, the optical image (on the left) shows the selected 500 µm x 500 µm domain of the silicon substrate. At that location, SEM images taken near the imprint area reveal the porous nature of the substrate from the center and towards the edge of the imprinted domains. Clearly, patterning has no fidelity in this case and pores are generated at the contact interface and on its surroundings.

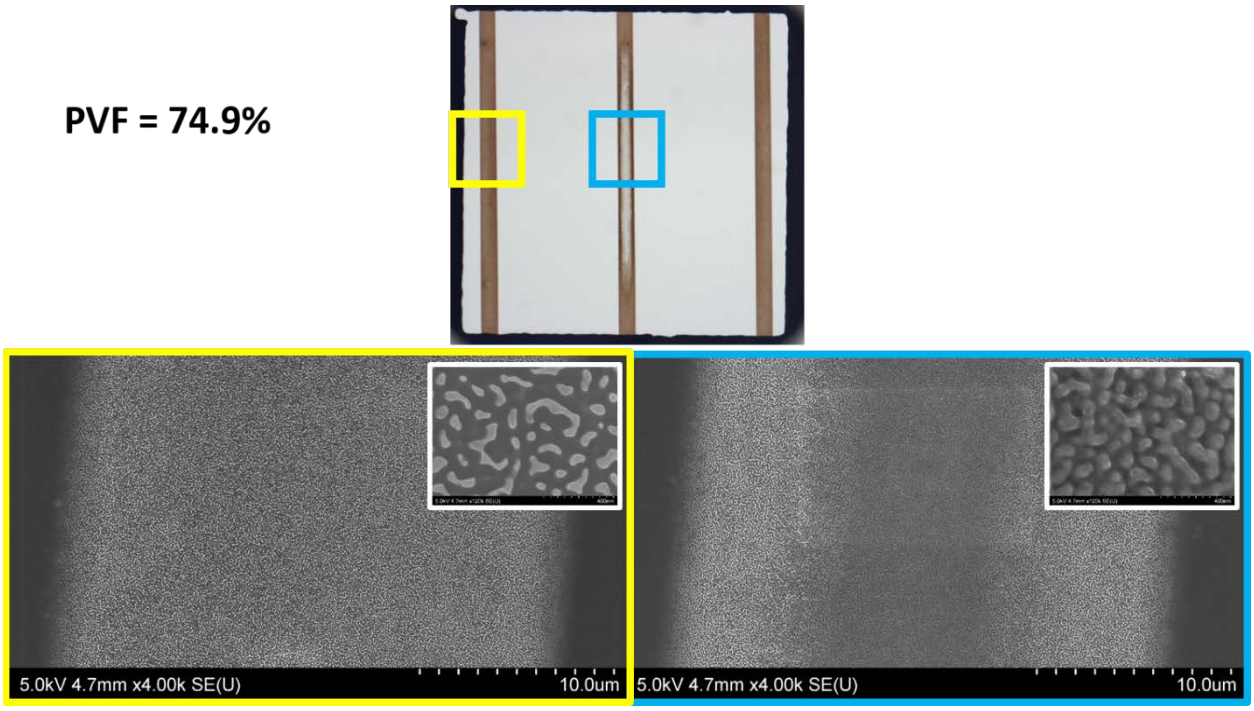


Figure 51: At the top row, the optical image (on the left) shows the selected 500 µm x 500 µm domain of the silicon substrate. At that location, SEM images taken near the imprint area reveal the porous nature of the substrate from the center and towards the edge of the imprinted domains. Clearly, patterning has no fidelity in this case and pores are generated at the contact interface and on its surroundings.

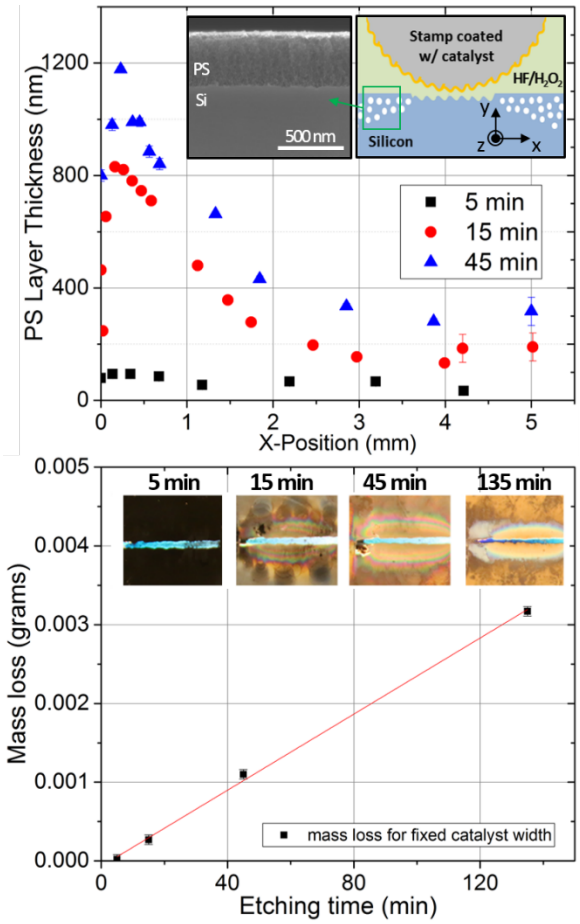


Figure 52: Characterization of the time evolution of imprinting with solid catalysts mounted onto roller stamps. As a function of time, the porous layer thickness (top graph) is measured via analysis of cross-section SEM images and recorded as a function of the distance from the contact edge. As the etching progresses the porous layer increases in thickness and the silicon total removed mass scales linearly with time (bottom graph).